EM78F811N

8-Bit

Microcontroller

Product Specification

DOC. VERSION 1.5

ELAN MICROELECTRONICS CORP.

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Specification Revision History

Doc. Version	Revision Description	Date
1.0	Initial version	2017/05/16
1.1	Modified title description on section 6.7	2017/08/21
1.2	1.Removed VIHX1 and VILX1 on DC electrical characteristics 2.Modified programming steps and demonstration programs on section 6.8.4	2017/10/20
1.3	1.Modified section 7.1 description 2.Removed SFR Bank 3 R8 in Figure 6-2 3.Modified Demonstration Programs on section 6.8.4	2018/02/27
1.4	1.Modified 6.1.28 Bank 2 R9 description 2.Modified Section 6.8.4 NOTE 3 description 3.Added item 4 on User Application Note	2018/11/19
1.5	Added UART peripheral	2021/07/28

User Application Note

(Before using this IC, take a look at the following description note, it includes important messages.)

1. When changing the IRC frequency from A-frequency to B-frequency, it will take some time for the MCU to start working. The expected waiting time corresponds to the B-frequency.
2. To obtain an accurate value, it is necessary to avoid any data transitions on the I/O pins during AD conversion.
3. The noise rejection function should always be disabled in Low Crystal Oscillator (LXT2) and Sleep mode.
4. AD pins that are not data-converted must be set as high-impedance input pins.

1 General Description

EM78F811N is an 8-bit microprocessor designed and developed with low-power, high-speed CMOS technology. It has an on-chip 1K×13-bit Electrical Flash Memory and a 128×8-bit in-system programmable EEPROM.

With its enhanced Flash-ROM features, EM78F811N provides a convenient way of developing and verifying user's programs. Moreover, this Flash-ROM device offers the advantage of easy and effective program updates, using development and programming tools. Users can avail of the ELAN Writer to easily program their development codes.

2 Features

- CPU configuration
  - 1K×13 bits on-chip Flash memory
  - 48×8 bits on-chip registers (SRAM)
  - 128 bytes in-system programmable EEPROM*
    Endurance: 100,000 write/erase cycles
  - More than 10 years data retention
  - 8-level stacks for subroutine nesting
  - Less than 1 mA at 5V / 4 MHz
  - Typically 11 μA, at 3V / 32kHz
  - Typically 1 μA, during sleep mode
- I/O port configuration
  - 3 bidirectional I/O ports: P5, P6, and P8
  - 14 I/O pins
  - Wake-up port : P6
  - High sink port : P6
  - 6 programmable pull-high I/O pins
  - 5 programmable pull-down I/O pins
  - 6 programmable open-drain I/O pins
  - External interrupt with Wake-up: P60
- Operating voltage range
  - 2.2V~5.5V at -40°C~85°C (Industrial)
- Operating frequency range (base on two clocks)
  - Crystal mode:
    DC~16 MHz @ 4V~5.5V
    DC~8 MHz @ 2.5V~5.5V
    DC~4 MHz @ 2.2V~5.5V
    DC~1 MHz @ 2.2V~5.5V
    DC~455 KHz @ 2.2V~5.5V
  - ERC mode:
    DC~10 KHz~1.75 MHz @ 3V~5.5V
  - IRC mode :
    DC~16 MHz @ 3V~5.5V;
    DC~8 MHz @ 2.5V~5.5V
    DC~4 MHz @ 2.2V~5.5V
    DC~1 MHz @ 2.2V~5.5V
    DC~455 KHz @ 2.2V~5.5V

Internal RC Frequency	Drift Rate (IRC Power is Regulator)			
	Temperature (-40°C~85°C)	Voltage (2.2V~5.5V)	Process	Total
4 MHz	± 3.75%		± 1%	± 4.75%
16 MHz	± 3.75%		± 1%	± 4.75%
8 MHz	± 3.75%		± 1%	± 4.75%
1 MHz	± 3.0%		± 1%	± 4%
455 KHz	± 3.0%		± 1%	± 4%

*The drift rate is based on NUWriter trim only, detail refer to DC Electrical Characteristics

- On-Chip Debug System (OCDS) with four breakpoints
- Eight available interrupts
  - Internal interrupt: 8
  - External interrupt: 3
- 6+1 channels Analog-to-Digital Converter with 12-bit resolution
  - Internal Vref: 2.048V/2.560V/3.072V/4.096V
  - One of the channels is 1/2 VDD power detection
- One set comparator with 4 to 1 CIN-
  Offset voltage: smaller than 2 mV
- One 8-bit Timer/Counter
  - TC3: Timer/Counter/PDO (programmable divider output)/PWM (pulse width modulation)
- One 16-bit Timer/Counter
  - TM1: Timer/Counter/PDO (programmable divider output)/PWM/Window/Buzzer/Capture
- Peripheral configuration
  - Universal asynchronous receiver / transmitter (UART) available
  - 8-bit real time clock only (TCC) with overflow interrupt
  - External interrupt input pin
  - 2/4/8/16 clocks per instruction cycle selected by code option
  - Power down (Sleep) mode
  - 3 programmable Level Voltage Reset
    LVR: 4.0V, 3.5V, 2.5V
- Single instruction cycle commands
- Special Features
  - Programmable free running Watchdog Timer
  - Power-on voltage detector available (1.9V ~ 2.0V)
- Package Type:
  - 10-pin MSOP 118mil : EM78F811NMS10
  - 14-pin SOP 150mil : EM78F811NSO14
  - 16-pin DIP 300mil : EM78F811NAD16
  - 16-pin SOP 150mil : EM78F811NASO16A

NOTE: *These are Green Products which do not contain hazardous substances*

3 Pin Assignment

3.1 10-Pin MSOP

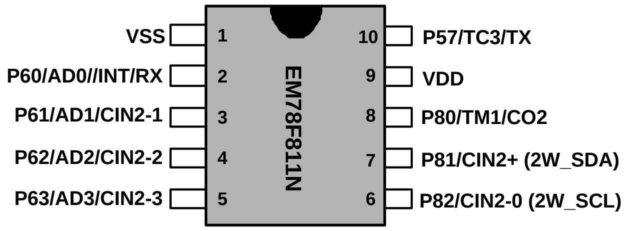


Figure 3-1a EM78F811NMS10

3.2 16-Pin DIP/SOP

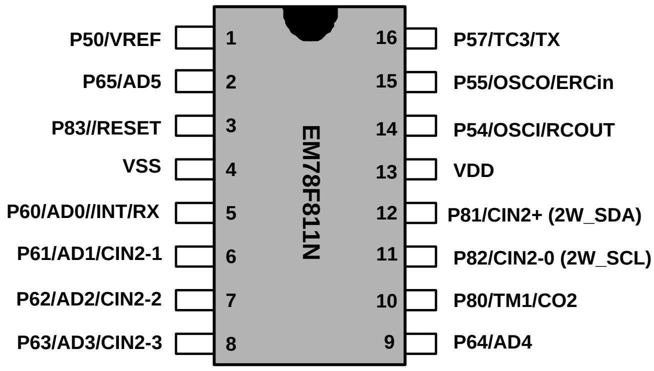


Figure 3-1b EM78F811NAD16 / EM78F811NASO16A

3.3 14-Pin SOP

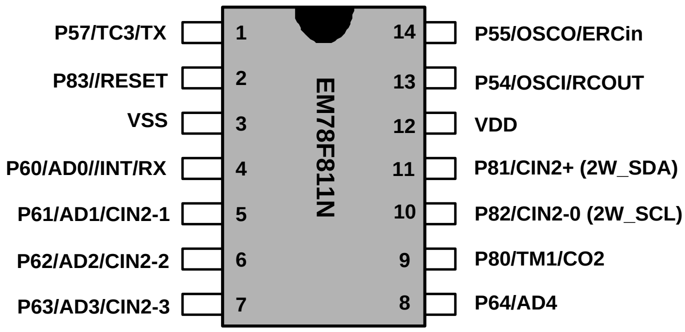


Figure 3-1c EM78F811NSO14

4 Pin Description

Legend: **ST:** *Schmitt Trigger input* **AN:** *Analog pin*
CMOS: *CMOS output* **XTAL:** *Oscillation pin for crystal/resonator*

Name	Function	Input Type	Output Type	Description
P50/VREF	P50	ST	CMOS	Bidirectional I/O pin with programmable pull-down
	VREF	AN	–	ADC external voltage reference
P54/OSCI/RCOUT	P54	ST	CMOS	Bidirectional I/O pin
	OSCI	XTAL	–	Clock input of crystal/resonator oscillator
	RCOUT	–	CMOS	Clock output of internal RC oscillator Clock output of external RC oscillator (open-drain)
P55/OSCO/ERCin	P55	ST	CMOS	Bidirectional I/O pin
	OSCO	–	XTAL	Clock output of crystal/resonator oscillator
	ERCin	AN	–	External RC input pin
P57/TC3/TX	P57	ST	CMOS	Bidirectional I/O pin
	TC3	ST	–	Timer 3 clock input (with PDO)
	TX	–	CMOS	UART transmit pin
P60/AD0//INT/RX	P60	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	AD0	AN	–	ADC Input 0
	/INT	ST	–	External interrupt pin
	RX	ST	–	UART receive pin
P61/AD1/CIN2-1	P61	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	AD1	AN	–	ADC Input 1
	CIN2-1	AN	–	Inverting end 1 of Comparator 2
P62/AD2/CIN2-2	P62	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	AD2	AN	–	ADC Input 2
	CIN2-2	AN	–	Inverting end 2 of Comparator 2
P63/AD3/CIN2-3	P63	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	AD3	AN	–	ADC Input 3
	CIN2-3	AN	–	Inverting end 3 of Comparator 2
P64/AD4	P64	ST	CMOS	Bidirectional I/O pin with programmable pull-high, open-drain, and pin change wake-up
	AD4	AN	–	ADC Input 4

(Continuation)

Name	Function	Input Type	Output Type	Description
P65/AD5	P65	ST	CMOS	Bidirectional I/O pin with programmable pull-high, open-drain, and pin change wake-up
	AD5	AN	–	ADC Input 5
P80/CO2/TM1	P80	ST	CMOS	Bidirectional I/O pin
	CO2	–	CMOS	Output of Comparator 2
	TM1	ST	–	Timer1 (16-bit) clock input (with PDO)
(2W_SDA)	**(2W_SDA)**	ST	CMOS	On Chip Debug System data pin
P81/CIN2+	P81	ST	CMOS	Bidirectional I/O pin
	CIN2+	AN	–	Non-inverting end of Comparator 2
(2W_SCL)	**(2W_SCL)**	ST	CMOS	On Chip Debug System clock pin
P82/CIN2-0	P82	ST	CMOS	Bidirectional I/O pin
	CIN2-0	AN	–	Inverting end of Comparator 2
P83//RESET	P83	ST	CMOS	Bidirectional I/O pin
	/RESET	ST	–	Internal pull-high reset pin
VDD	VDD	Power	–	Power
VSS	VSS	Power	–	Ground

NOTE:
Pin priority: Analog > Digital > I/O

5 System Overview

5.1 Memory Map

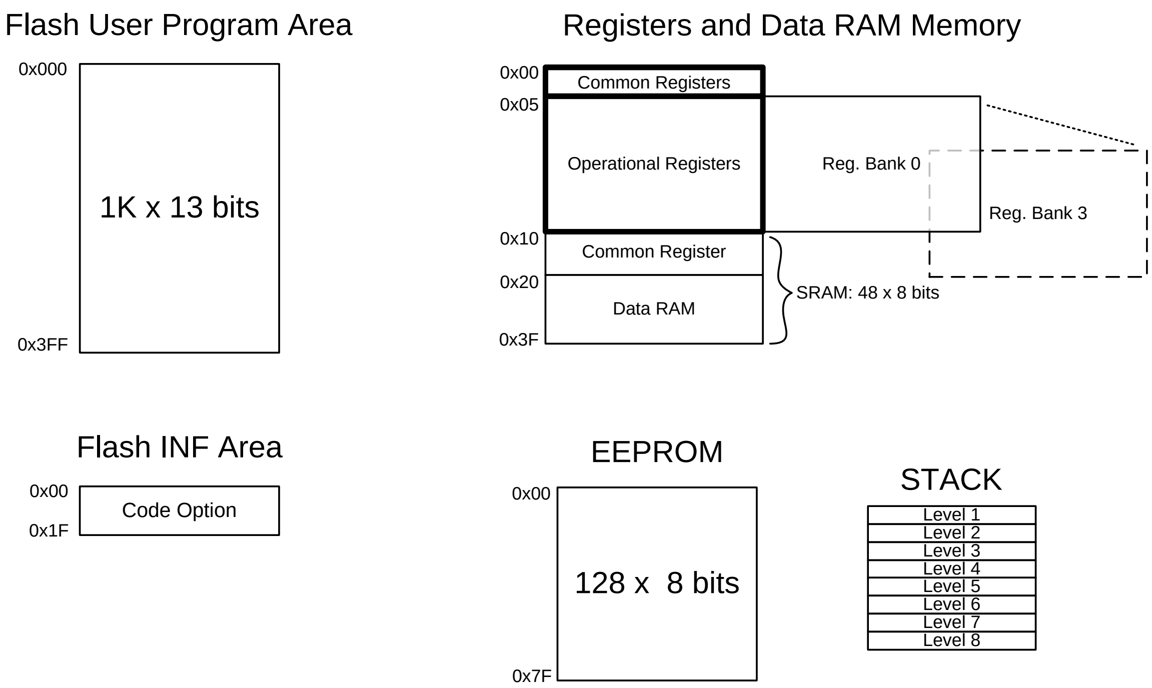


Figure 5-1 Memory Map

Notes:

1. Flash User Program Area is protected when power down occurs, and will not be read, written and erased from the OCDS.
2. EEPROM can be protected by Code Option Word0<2~0>, and will not be read from the OCDS.

5.2 Block Diagram

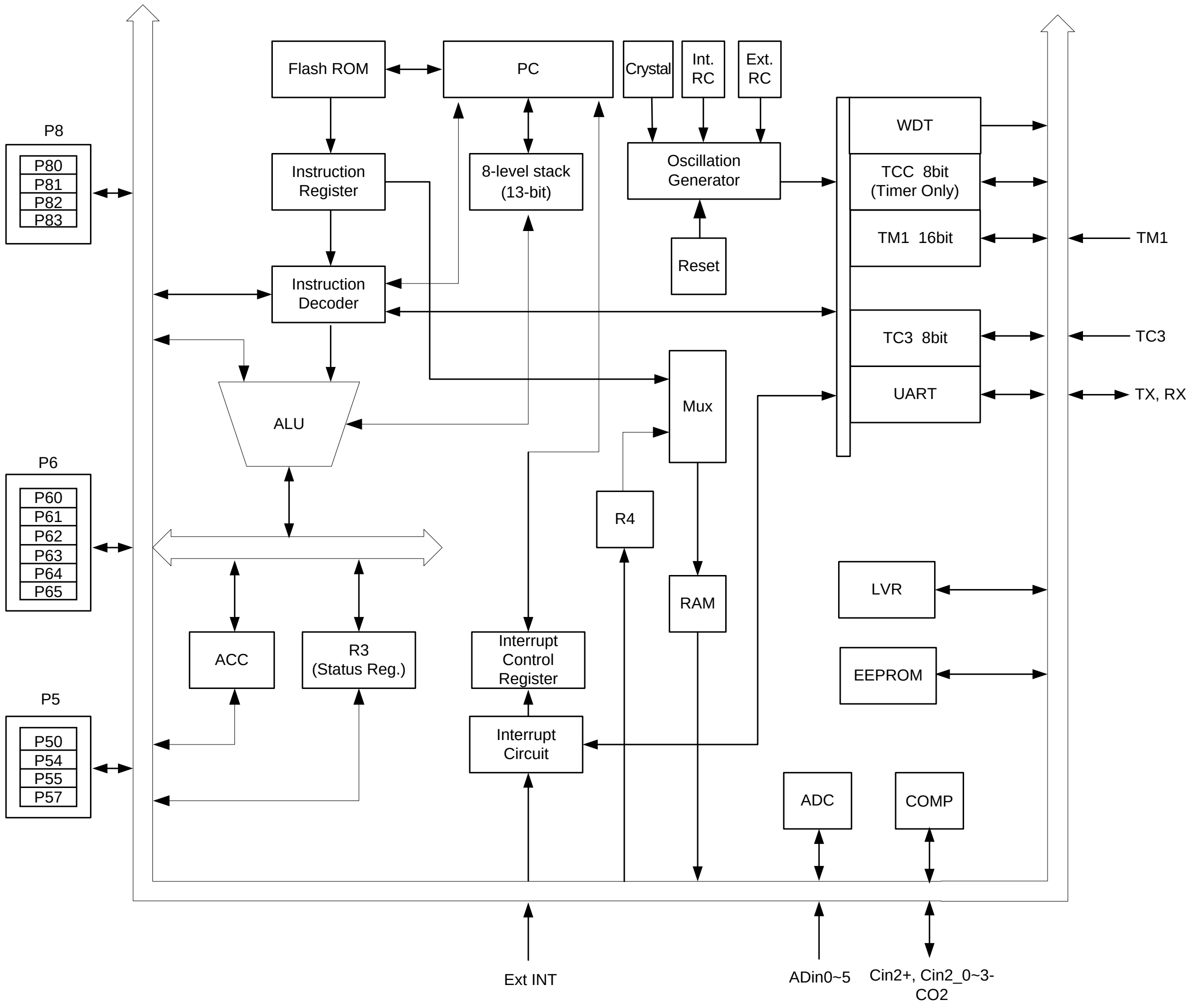


Figure 5-2 Functional Block Diagram

6 Functional Description

6.1 Operational Registers

6.1.1 R0: IAR (Indirect Addressing Register)

R0 is not a physically implemented register. It is used as an indirect addressing pointer. Any instruction using R0 as a pointer actually accesses data pointed by the RAM Select Register (R4).

6.1.2 R1: TCC (Timer Clock)

R1 is incremented by the instruction cycle clock. It is writable and readable as any other registers. It is defined by resetting PSTE (CONT-3).

The prescaler is assigned to TCC if the PSTE bit (CONT-3) is reset. The content of the prescaler counter is cleared only when the TCC register is written with a value.

6.1.3 R2: PC (Program Counter and Stack)

Depending on the device type, R2 and hardware stack are 10-bit wide. The structure is depicted in Figure 6-1 below.

The configuration structure generates 1K×13 bits on-chip Flash ROM addresses to the relative programming instruction codes. One program page is 1024 words long.

R2 is set as all "**0**"s when under a reset condition.

"JMP" instruction allows direct loading of the lower 10 program counter bits. Thus, "JMP" allows the PC to go to any location within a page.

"CALL" instruction loads the lower 10 bits of the PC, and PC+1 are pushed onto the stack. Thus, the subroutine entry address can be located anywhere within a page.

"RET" ("RETL k", "RETI") instruction loads the program counter with the contents of the top-level stack.

"ADD R2, A" allows a relative address to be added to the current PC, and the ninth and above bits of the PC will increase progressively.

"MOV R2, A" allows the loading of an address from the "A" register to the lower 8 bits of the PC, and the ninth and tenth bits of the PC remain unchanged.

Any instruction except “ADD R2,A”, which is written to R2 (e.g., "MOV R2, A", "BC R2, 6"), will cause the ninth bit and the tenth bit (A8~A9) of the PC to remain unchanged.

All instructions are single instruction cycle (fclk/2, fclk/4, fclk/8, or fclk/16) except for the instruction that would change the contents of R2 and “TBRD” instruction. The “TBRD” instructions need two instruction cycles.

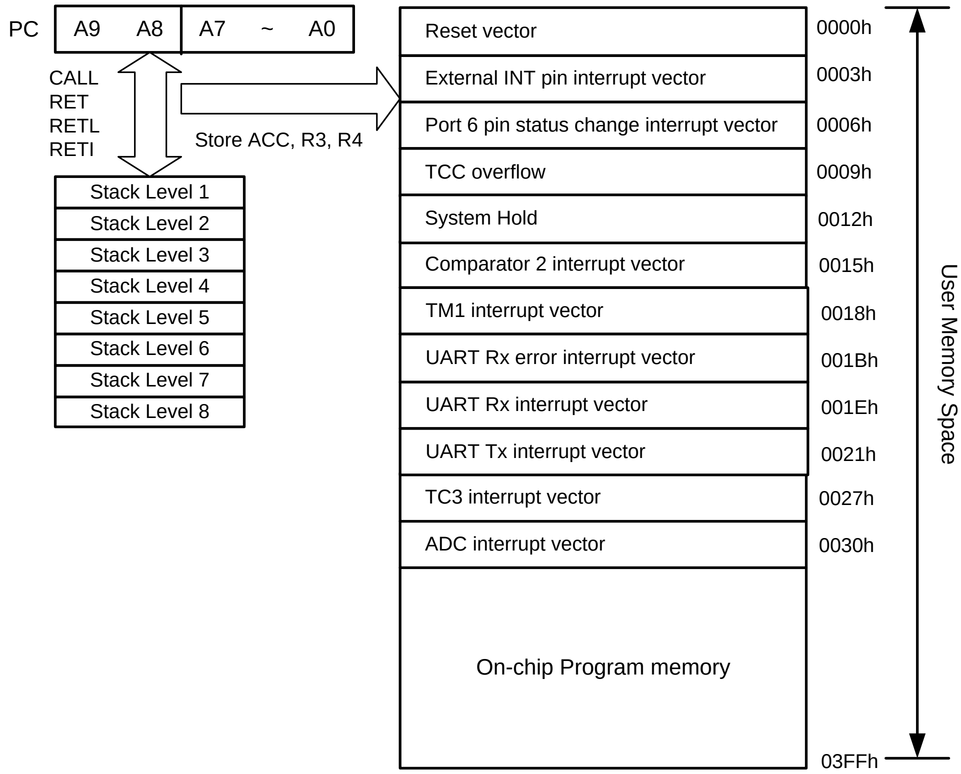


Figure 6-1 Program Counter Organization

Address	Register Bank 0	Register Bank 1	Register Bank 2	Register Bank 3	Control Register
01	R1 (TCC)				
02	R2 (PC)				
03	R3 (SR)				
04	R4 (RSR)	R4(7,6) (0,1)	(1,0)	(1,1)	
05	R5 (PORT5)	R5 (Reserved)	R5 (AISR)	R5 (Reserved)	IOC5 (IOCR5)
06	R6 (PORT6)	R6 (Reserved)	R6 ADCON	R6 (TBHP)	IOC6 (IOCR6)
07	R7 (Reserved)	R7 (Reserved)	R7 (ADCON2)	R7 (CMP2CON)	IOC7 (Reserved)
08	R8 (PORT8)	R8 (IRCS)	R8 ADDH	R8 (Reserved)	IOC8 (IOCR8)
09	R9 (TBLP)	R9 (TM1CR1)	R9 (ADDL)	R9 (Reserved)	IOC9 (Reserved)
0A	RA (WUPC)	RA (TM1CR2)	RA (URCR)	RA (Reserved)	IOCA (WDTCR)
0B	RB (EECR)	RB (TM1DAH)	RB (URS)	RB (Reserved)	IOCB (P6PDCR)
0C	RC (EEPA)	RC (TM1DBH)	RC (URTD)	RC (Reserved)	IOCC (P6ODCR)
0D	RD (EEPD)	RD (TM1DBH)	RD (URRDL)	RD (TC3CR)	IOCD (P6PHCR)
0E	RE (OMCR)	RE (TM1DBL)	RE (URRDH)	RE (TC3D)	IOCE (IMR2)
0F	RF (ISR1)	RF (ISR2)	RF (Reserved)	RF (Reserved)	IOCF (IMR1)
10 : 1F	16-Byte Common Register				
20 : 3F	Bank 0 32x8				

Figure 6-2 Data Memory Configuration

6.1.4 R3: SR (Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	T	P	Z	DC	C

Bits 7 ~ 5 Not used, set to "**0**" all the time

Bit 4 (T): Time-out bit

Set to "**1**" with the "SLEP" and "WDTC" commands, or during power up and reset to "**0**" by WDT time-out.

Bit 3 (P): Power down bit

Set to 1 during power-on or by a "WDTC" command and reset to "0" by a "SLEP" command.

Bit 2 (Z): Zero flag

Set to "**1**" if the result of an arithmetic or logic operation is zero.

Bit 1 (DC): Auxiliary carry flag

Bit 0 (C): Carry flag

C is set when a carry occurs and cleared when a borrow occurs during an arithmetic operation. The set and clear of the Carry Flag depends on the operation performed.

For ADD, INC, INCA instructions

0: No carry occurs.

1: Carry occurs.

For SUB, DEC, DECA, instructions

0: Borrow occurs.

1: No borrow occurs.

For RLC, RRC, RLCA, RRCA instructions

The Carry flag is used as a link between the least significant bit (LSB) and the most significant bit (MSB).

6.1.5 R4: RSR (RAM Select Register)

Bits 7 ~ 6: These are used to select Bank 0 ~ Bank 3

Bits 5 ~ 0: These are used to select registers (Address: 00~3F) in indirect addressing mode. See the data memory configuration in Figure 6-2 above.

6.1.6 Bank 0 R5 ~ R6, R8 (Port 5 ~ Port 6, Port 8)

R5 ~ R6, and R8 are I/O registers.

6.1.7 Bank 0 R9: TBLP (Table Point Register for Instruction TBRD)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RBit7	RBit6	RBit5	RBit4	RBit3	RBit2	RBit1	RBit0

Bits 7 ~ 0: These are the least 8 significant bits of address for program code.

NOTES:

1. Bank 0 R9 overflow will carry to Bank 3 R6.

2. Bank 0 R9 underflow will borrow from Bank 3 R6.

6.1.8 Bank 0 RA: WUPC (Wake-up Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMP2WE	ICWE	ADWE	EXWE	URWE	-	-	-

Bit 7 (CMP2WE): Comparator 2 wake-up enable bit.

0: Disable Comparator 2 wake-up

1: Enable Comparator 2 wake-up

When the Comparator 2 output status change is used to enter an interrupt vector or to wake-up the EM78F811N from Sleep mode, the CMP2WE bit must be set to "Enable".

Bit 6 (ICWE): Port 6 input status change wake-up enable bit

0: Disable Port 6 input status change wake-up

1: Enable Port 6 input status change wake-up

Bit 5 (ADWE): ADC wake-up enable bit

0: Disable ADC wake-up

1: Enable ADC wake-up

When ADC Complete is used to enter an interrupt vector or to wake-up the EM78F811N from sleep with AD conversion running, the ADWE bit must be set to "Enable".

Bit 4 (EXWE): External /INT wake-up enable bit

0: Disable External /INT pin wake-up

1: Enable External /INT pin wake-up

Bit 3 (URWE): UART wake-up enable bit

0: Disable UART wake-up

1: Enable UART pin wake-up

When URWE is set to enable, UART can wake up MCU from IDLE mode to Normal mode but Fm will not stop at IDLE mode.

Bits 2 ~ 0: Not used, set to "**0**" all the time

6.1.9 Bank 0 RB: EECR (EEPROM Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RD	WR	EEWE	EEDF	EEPC	-	-	-

Bit 7 (RD): Read control register

0: Does not execute EEPROM read

1: Read EEPROM contents (RD can be set by software, and cleared by hardware after Read instruction is completed).

Bit 6 (WR): Write control register

0: Write cycle to the EEPROM is completed.

1: Initiate a write cycle (WR can be set by software, and cleared by hardware after Write cycle is completed).

Bit 5 (EEWE): EEPROM Write Enable bit.

0: Prohibit write to the EEPROM

1: Allow EEPROM write cycles

Bit 4 (EEDF): EEPROM Detect Flag

0: Write cycle is completed.

1: Write cycle is unfinished.

Bit 3 (EEPC): EEPROM power-down control bit

0: Switch off the EEPROM

1: EEPROM is operating

Bits 2 ~ 0: Not used, set to “**0**” all the time

6.1.10 Bank 0 RC: EEPA (128 Bytes EEPROM Address)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	EE_A6	EE_A5	EE_A4	EE_A3	EE_A2	EE_A1	EE_A0

Bits 6 ~ 0: 128 bytes EEPROM address

6.1.11 Bank 0 RD: EEPD (128 Bytes EEPROM Data)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EE_D7	EE_D6	EE_D5	EE_D4	EE_D3	EE_D2	EE_D1	EE_D0

Bits 7 ~ 0: 128 bytes EEPROM data

6.1.12 Bank 0 RE: OMCR (Mode Select Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PERCS	TIMERSC	CPUS	IDLE	-	-	-	-

Bit 7 (PERCS): Periphery Clock Source for Green and Idle modes.

0: Fm will be Stop in Green and Idle modes.

1: Fm will be oscillated in Green and Idle modes.

Bit 6 (TIMERSC): TCC, TC3 Clock Source Select

0: Fs is used as Fc

1: Fm is used as Fc

Bit 5 (CPUS): CPU Oscillator Source Select

0: Fs**:** Sub frequency for WDT internal RC time base

1: Fm**:** Main-oscillator clock

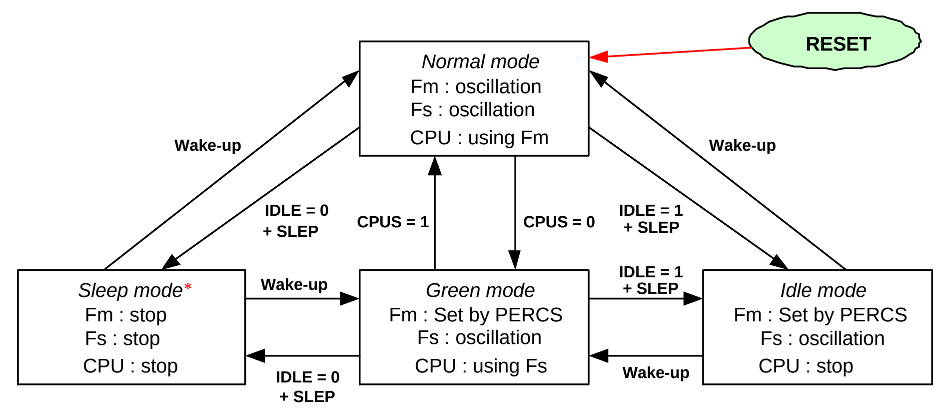
When CPUS=0, the CPU oscillator selects a sub-oscillator and the main oscillator is stopped.

Bit 4 (IDLE): Idle Mode Enable Bit

0: IDLE="**0**" + SLEP instruction → Sleep mode

1: IDLE="**1**" + SLEP instruction → Idle mode

■ **CPU Operation Mode**



Note: * <u>*Only when WDT IRC is Fs.*</u>

If the watchdog function is enabled before going into Sleep mode, Fs does not stop. Hence, some circuits, like timer/counter (of which clock source is Fs) must be disabled before going into Sleep mode, especially when the corresponding interrupt is enabled.

Figure 6-3 CPU Operation Mode

WSTO: Waiting Time from Start-to-Oscillation for Fs, N: Normal mode, G: Green mode, S: Sleep mode, I: Idle mode.
POR: Power-On Reset, LVR: Low voltage Reset, EXR: External Reset (Reset Pin), WDT: Watchdog Reset.
16ms: The time is 256/16KHz and Latch Code Option at 12ms.

Fm	Fs	POR / LVR	EXR / WDT					
			N	S	G	G	I	I
					PERCS = 1	PERCS = 0	PERCS = 1	PERCS = 0
IRC	IRC	WSTO+16ms+ 8/Fs[1]	16ms+8/Fs[1]	WSTO+16ms+ 8/Fs[1]	16ms+8/Fs[1]	16ms+8/Fs[1]	16ms+8/Fs[1]	16ms+8/Fs[1]
Crystal		WSTO+16ms+ 510/Fm	16ms+ 510/Fm	WSTO+16ms+ 510/Fm	16ms+ 510/Fm	16ms+ 510/Fm	16ms+ 510/Fm	16ms+ 510/Fm
ERC		WSTO+16ms+ 8/Fm	16ms+ 8/Fm	WSTO+16ms+ 8/Fm	16ms+ 8/Fm	16ms+ 8/Fm	16ms+ 8/Fm	16ms+ 8/Fm

Table 6-1 Warm-up Time from Reset Condition

WSTO: Waiting Time from Start-to-Oscillation, N: Normal mode, G: Green mode, S: Sleep mode, I: Idle mode.

Fm	Fs	G → N		I → N		S → N
		PERCS = 1	PERCS = 0	PERCS = 1	PERCS = 0	
IRC	IRC	8/Fs[1]	8/Fs[1]	8/Fs[1]	(2/3/4/8)/Fs[1]	WSTO+ 8/Fs[1]
Crystal		510/Fm	WSTO+ 510/Fm	510/Fm	WSTO+ 510/Fm	WSTO+ 510/Fm
ERC		8/Fm	WSTO+ 8//Fm	8/Fm	WSTO+ 8/Fm	WSTO+ 8/Fm
Fm	**Fs**	**I → G**		**I → G**		**S → G**
		PERCS = 1		**PERCS = 0**		
IRC/Crystal/ERC	IRC	2/Fs		2/Fs		WSTO+ 32/Fs

Table 6-2 Warm-up Time During Mode Change

> **Note:**
> [1]: The Fs is only 128KHz (SFS is invalid)

Bits 3 ~ 0: Not used, set to "**0**" all the time

6.1.13 Bank 0 RF: ISR1 (Interrupt Status Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SHIF	ADIF	-	-	-	EXIF	ICIF	TCIF

***NOTE:** "**1**" means with interrupt request "**0**" means no interrupt occurs*

Bit 7 (SHSF): System hold interrupt flag, this flag must be cleared by software.

Bit 6 (ADIF): Interrupt flag for analog to digital conversion. Set when AD conversion is completed, reset by software.

Bits 5 ~ 3: Not used, set to "**0**" all the time

Bit 2 (EXIF): External interrupt flag. Set by a falling edge on the /INT pin, reset by software.

Bit 1 (ICIF): Port 6 input status change interrupt flag. Set when Port 6 input changes, reset by software.

Bit 0 (TCIF): TCC overflow interrupt flag. Set when TCC overflows, reset by software.

NOTES:

1. RF can be cleared by instruction but cannot be set.

2. IOCF is an interrupt mask register.

3. The result of reading RF is the "Logic AND" of RF and IOCF.

4. These flags are set by hardware and must be cleared by software.

6.1.14 R10 ~ R3F

These are all 8-bit general-purpose registers.

6.1.15 Bank 1 R5~R7

These are reserved registers.

6.1.16 Bank 1 R8 (IRC Select Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RCM1	RCM0	RCM2	-	-	-	-	-

Bits 7 ~ 5 (RCM2 ~ RCM0): IRC mode select bits. Bank 1 R8<7, 6, 5> is enabled when Word 1<12> COBS0 = "1".

RCM2	RCM1	RCM0	Frequency (Hz)
0	0	0	4M
0	0	1	16M
0	1	0	8M
0	1	1	455K
1	x	x	1M

NOTES:

1. The initial values of Bank1 R8<7, 6, 5> will be kept the same as Word 1<4, 3, 2>.

2. If user changes the IRC frequency from A-frequency to B-frequency, it will take some time for the MCU to work. The waiting time corresponds to the B-frequency.

6.1.17 Bank 1 R9: TM1CR1 (Timer/Counter 1 Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM1S	TM1RC	TM1SS1	TM1SS0	TM1FF	TM1MOS	TM1IS1	TM1IS0

Bit 7 (TM1S): Timer/Counter 1 start control.

0: Stop and clear counter.

1: Start.

Bit 6 (TM1RC): Timer 1 Read Control Bit.

0: When set to 0, data cannot be read from TM1DB.

1: When set to 1, data read from TM1DB is a number of counting.

Bit 5 (TM1SS1): Timer/Counter 1 clock source select bit1.

0: Internal clock as count source (Fc)- Fs/Fm.

1: External TM1 pin as count source (Fc). It is used only in timer/counter mode.

Bit 4 (TM1SS0): Timer/Counter 1 clock source selection bit.

0: The Fs is used as count source (Fc).

1: The Fm is used as count source (Fc).

Bit 3 (TM1FF): Inversion for Timer/Counter 1 as PWM or PDO mode

0: Duty is logic 1.

1: Duty is logic 0.

Bit 2 (TM1MOS): Timer Output Mode Select Bit.

0: Repeating mode.

1: One–shot mode.

NOTES:

1. One-shot mode means the timer only counts a cycle.

2. One-shot is invalid in Buzzer mode.

Bits 1~0 (TM1IS1~0): Timer 1 Interrupt Type Select Bits. These two bits are used when the Timer operates in PWM and Capture modes.

TM1IS1	TM1IS0	Timer 1 Interrupt Type Select
0	0	TM1DA(period) matching
0	1	TM1DB(duty) matching
1	x	TM1DA and TM1DB matching

6.1.18 Bank 1 RA: TM1CR2 (Timer/Counter 1 Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM1M2	TM1M1	TM1M0	-	TM1CK3	TM1CK2	TM1CK1	TM1CK0

Bits 7~5 (TM1M2~0): Timer/Counter 1 operation mode select.

TM1M2	TM1M1	TM1M0	Operating Mode Select
0	0	0	Timer/Counter Rising Edge
0	0	1	Timer/Counter Falling Edge
0	1	0	Capture Mode Rising Edge*
0	1	1	Capture Mode Falling Edge*
1	0	0	Window mode
1	0	1	Programmable Divider output
1	1	0	Pulse Width Modulation output
1	1	1	Buzzer (output timer/counter clock source. The duty cycle of clock source must be 50/.50)

Bit 4: Not used, set to "**0**" all the time

Bits 3~0 (TM1CK3~0): Timer/Counter 1 clock source prescaler select.

TM1CK3	TM1CK2	TM1CK1	TM1CK0	Clock Source	Resolution 8MHZ	Max time 8MHz	Resolution 16KHZ	Max time 16KHz
				Normal	FC=8M	FC=8M	FC=16K	FC=16K
0	0	0	0	F_C	125ns	32us	62.5us	16ms
0	0	0	1	$F_C/2$	250ns	64us	125us	32ms
0	0	1	0	$F_C/2^2$	500ns	128us	250us	64ms
0	0	1	1	$F_C/2^3$	1us	256us	500us	128ms
0	1	0	0	$F_C/2^4$	2us	512us	1ms	256ms
0	1	0	1	$F_C/2^5$	4us	1024us	2ms	512ms
0	1	1	0	$F_C/2^6$	8us	2048us	4ms	1024ms
0	1	1	1	$F_C/2^7$	16us	4096us	8ms	2048ms
1	0	0	0	$F_C/2^8$	32us	8192us	16ms	4096ms
1	0	0	1	$F_C/2^9$	64us	16384us	32ms	8192ms
1	0	1	0	$F_C/2^{10}$	128us	32768us	64ms	16384ms
1	0	1	1	$F_C/2^{11}$	256us	65536us	128ms	32768ms
1	1	0	0	$F_C/2^{12}$	512us	131072us	256ms	65536ms
1	1	0	1	$F_C/2^{13}$	1.024ms	262144us	512ms	131072ms
1	1	1	0	$F_C/2^{14}$	2.048ms	524.288ms	1.024s	262144ms
1	1	1	1	$F_C/2^{15}$	4.096ms	1.048s	2.048s	524288ms

6.1.19 Bank 1 RB: TM1DAH (High Byte Timer/Counter 1 Data Buffer A)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM1DAH7	TM1DAH6	TM1DAH5	TM1DAH4	TM1DAH3	TM1DAH2	TM1DAH1	TM1DAH0

Bits 7~0 (TM1DAH7~0): Data buffer A High Byte of 16 bit timer/counter 1.

6.1.20 Bank 1 RC: TM1DAL (Low Byte Timer/Counter 1 Data Buffer A)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM1DAL7	TM1DAL6	TM1DAL5	TM1DAL4	TM1DAL3	TM1DAL2	TM1DAL1	TM1DAL0

Bits 7~0 (TM1DAL7~0): Data buffer A Low Byte of 16 bit timer/counter 1.

6.1.21 Bank 1 RD: TM1DBH (High Byte Timer/Counter 1 Data Buffer B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM1DBH7	TM1DBH6	TM1DBH5	TM1DBH4	TM1DBH3	TM1DBH2	TM1DBH1	TM1DBH0

Bits 7~0 (TM1DAL7~0): Data buffer B High Byte of 16 bit timer/counter 1.

6.1.22 Bank 1 RE: TM1DBL (Low Byte Timer/Counter 1 Data Buffer B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM1DBL7	TM1DBL6	TM1DBL5	TM1DBL4	TM1DBL3	TM1DBL2	TM1DBL1	TM1DBL0

Bits 7~0 (TM1DAL7~0): Data buffer B Low Byte of 16 bit timer/counter 1.

NOTE:

The period value set by users is extra plus 1 in inner circuit.

For example:

If the period value is set as 0x4F, the circuit actually processes 0x50 period length.

If the period value is set as 0xFF, the circuit actually processes 0x100 period length.

6.1.23 Bank 1 RF: ISR2 (Interrupt Status Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMP2IF	-	TC3IF	TM1DBSF	TM1DASF	UERRIF	URIF	UTIF

Bit 7 (CMP2IF): Comparator 2 Interrupt Flag. Set when a change occurs in the Comparator 2 output, reset by software.

Bit 6: Not used, set to "**0**" all the time.

Bit 5 (TC3IF): 8-bit Timer/Counter 3 Interrupt Flag.

Bit 4 (TM1DBSF): 16-bit Timer/Counter 1 duty status Flag. Can be cleared by software.

Bit 3 (TM1DASF): 16-bit Timer/Counter 1 period status Flag. Can be cleared by software.

Bit 2 (UERRIF): UART receiving error interrupt flag, this flag can be cleared by software or UART disabled

Bit 1 (URIF): UART receive interrupt flag, this flag can be cleared by software.

Bit 0 (UTIF): UART transmit interrupt flag, this flag can be cleared by software.

NOTE:
These flags are set by hardware and must be cleared by software.

6.1.24 Bank 2 R5: AISR (ADC Input Select Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0

The AISR register individually defines the Port 6 pins as analog input or digital I/O.

Bits 7 ~ 6: Not used, set to "**0**" all the time.

Bit 5 (ADE5): AD converter enable bit of P65 pin.

0: Disable ADC5, P65 functions as I/O pin.

1: Enable ADC5 to function as analog input pin.

Bit 4 (ADE4): AD converter enable bit of P64 pin.

0: Disable ADC4, P64 acts as I/O pin.

1: Enable ADC4 to acts as analog input pin.

Bit 3 (ADE3): AD converter enable bit of P63 pin.

0: Disable ADC3, P63 acts as I/O pin.

1: Enable ADC3 to acts as analog input pin.

Bit 2 (ADE2): AD converter enable bit of P62 pin.

0: Disable ADC2, P62 acts as I/O pin.

1: Enable ADC2 to acts as analog input pin.

Bit 1 (ADE1): AD converter enable bit of P61 pin.

0: Disable ADC1, P61 acts as I/O pin.

1: Enable ADC1 to acts as analog input pin.

Bit 0 (ADE0): AD converter enable bit of P60 pin.

0: Disable ADC0, P60 acts as I/O pin.

1: Enable ADC0 to acts as analog input pin.

The following chart shows the priority of P60/ADC0//INT.

P60 / ADC0 / /INT Pin Priority		
High	Medium	Low
/INT	ADC0	P60

6.1.25 Bank 2 R6: ADCON (A/D Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CKR2	CKR1	CKR0	ADRUN	ADPD	ADIS2	ADIS1	ADIS0

Bit 7 ~ Bit 5 (CKR2 ~ CKR0): Prescaler of ADC oscillator clock rate

CKR2	CKR1	CKR0	Operating Clock
0	0	0	Fosc/4
0	0	1	Fosc/16
0	1	0	Fosc
0	1	1	Fosc/2
1	x	x	Fosc/8

Bit 4 (ADRUN): ADC starts to run

0: Reset when AD conversion is completed. This bit cannot be reset by software.

1: AD conversion started. This bit can be set by software.

Bit 3 (ADPD): ADC Power-down mode

0: ADC is disabled. ADC is in low power shutdown.

1: ADC is enabled. ADC is active and ready for data conversions.

Bits 2 ~ 0 (ADIS2~ADIS0): Analog Input Select

ADIS2	ADIS1	ADIS0	ADC Input Pin
0	0	0	AD0
0	0	1	AD1
0	1	0	AD2
0	1	1	AD3
1	0	0	AD4
1	0	1	AD5
1	1	0	1/2VDD
1	1	1	X

The following table shows the priority of P50/VREF pins. The pins can only be changed when the ADIF bit and the ADRUN bit are both low.

P50/VREF Pin Priority	
High	Low
VREF	P50

6.1.26 Bank 2 R7: ADCON2 (A/D Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADLPFEN	-	-	IRVS2	IRVS1	IRVS0	SHS1	SHS0

Bit 7 (ADLPFEN): Low pass filter of ADC for internal voltage reference is enabled.

Bits 6 ~ 5: Not used, set to "**0**" all the time

Bit 4~2 (IRVS2~0): Internal Reference Voltage Selection.

IRVS2	IRVS1	IRVS0	Reference Voltage
0	0	0	VDD (P50 is I/O)
0	0	1	4.096 V
0	1	0	3.072 V
0	1	1	2.560 V
1	0	0	2.048 V
1	0	1	VREF
1	1	0	VREF
1	1	1	VREF

Bits 1~0 (SHS1~0): Sample and Hold Timing Select.

SHS1	SHS0	Sample and Hold Timing
0	0	2 x T_{AD}
0	1	4 x T_{AD}
1	0	8 x T_{AD}
1	1	12 x T_{AD}

T_{AD}: Period of ADC Operating Clock

NOTES:

Sample and Hold Timing specification:

1. Recommend at least 4 µs when VDD is between 3.0V~5.5V.

2 .Recommend at least 16 µs when VDD is between 2.5V~5.5V.

6.1.27 Bank 2 R8: ADDH (AD High 8-Bit Data Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4

When AD conversion is completed, the result of high 8-bit is loaded into the ADDH. The ADRUN bit is cleared, and the ADIF is set. R8 is read only.

6.1.28 Bank 2 R9: ADDL (AD Low 4-Bit Data Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	AD3	AD2	AD1	AD0

Bits 7 ~ 4: Unimplemented, read as ‘**0**’

Bits 3 ~ 0 (AD3~AD0): AD low 4-bit data buffer. R9 is read only.

6.1.29 Bank 2 RA: URCR (UART Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
UINVEN	UMODE1	UMODE0	BRATE2	BRATE1	BRATE0	UTBF	TXE

Bit 7 (UINVEN): Enable UART TXD and RXD Port Inverse Output Bit

0: Disable TXD and RXD port inverse output.

1: Enable TXD and RXD port inverse output.

Bits 6~5 (UMODE1~UMODE0): UART mode select bits

UMODE1	UMODE0	UART mode
0	0	7-bit
0	1	8-bit
1	0	9-bit
1	1	Reserved

Bits 4~2 (BRAT2~BRAT0): transmit Baud rate selection

BRATE2	BRATE1	BRATE0	$F_{UARTCLK}$	Baud Rate (Fc=1Mhz)	Baud Rate (Fc=4Mhz)	Baud Rate (Fc=8Mhz)	Baud Rate (Fc=16Mhz)
0	0	0	Fc/1	38400			
0	0	1	Fc/2	19200			
0	1	0	Fc/4	9600	38400		
0	1	1	Fc/8	4800	19200	38400	
1	0	0	Fc/16	2400	9600	19200	38400
1	0	1	Fc/32	1200	4800	9600	19200
1	1	0	Fc/64		2400	4800	9600
1	1	1	$TC3_{MATCH}$ / 2		1200 (TC3D=64)	2400 (TC3D=64) 1200 (TC3D=128)	4800 (TC3D=64) 2400 (TC3D=128)

Notes:

1. **If BRAT2~0 is 000~110:**

$$UART\ one\ bit\ cycle = T_{UARTCLK} \times 26 \quad \Rightarrow Baud\ \ Rate = \frac{1}{T_{UARTCLK} \times 26} = \frac{F_{UARTCLK}}{26}$$

2. **If BRAT2~0 is 111:**

$$Baud\ \ Rate = \frac{F_{UARTCLK}}{26} = \frac{TC3_{MATCH}}{2 \times 26} = \frac{Fc}{TC3D \times 2 \times 26} \quad \Rightarrow TC3D = \frac{Fc}{Baud\ \ Rate \times 2 \times 26}$$

Bit 1 (UTBF): UART transfer buffer empty flag. Set to 1 when transfer buffer is empty. Reset to 0 automatically when write into URTD register. UTBF bit will be clear by hardware when enabling transmission. And UTBF bit is read-only. Therefore, write URTD register is necessary when want to start transmitting shifting.

Bit 0 (TXE): Enable transmission

0: Disable

1: Enable

6.1.30 Bank 2 RB: URS (UART Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
URTD8	EVEN	PRE	PRERR	OVERR	FMERR	URBF	RXE

Bit 7 (URTD8): UART transmit data bit 8. Write only.

Bit 6 (EVEN): select parity check

0: Odd parity

1: Even parity

Bit 5 (PRE): enable parity addition

0: Disable

1: Enable

Bit 4 (PRERR): Parity error flag. Set to 1 when parity error happened, and clear to 0 by software.

Bit 3 (OVERR): Over running error flag. Set to 1 when overrun error happened, and clear to 0 by software.

Bit 2 (FMERR): Framing error flag. Set to 1 when framing error happen, and clear to 0 by software.

Bit 1 (URBF): UART read buffer full flag. Set to 1 when one character is received. Reset to 0 automatically when read from URRDL register. URBF will be clear by hardware when enabling receiving. And URBF bit is read-only. Therefore, read URRDL register is necessary to avoid overrun error.

Bit 0 (RXE): Enable receiving

0: Disable

1: Enable

6.1.31 Bank 2 RC: URTD (UART Transmit Data Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
URTD7	URTD6	URTD5	URTD4	URTD3	URTD2	URTD1	URTD0

Bits 7~0 (URTD7~URTD0): UART transmit data buffer. Write only.

6.1.32 Bank 2 RD: URRDL (UART Receive Data Low Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
URRD7	URRD6	URRD5	URRD4	URRD3	URRD2	URRD1	URRD0

Bits 7~0 (URRDL7~0): UART Receive Data Buffer. Read only.

6.1.33 Bank 2 RE: URRDH (UART Receive Data High Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
URRD8	-	-	-	-	-	-	URSS

Bit 7 (URRD8): UART receive data bit 8. Read only.

Bits 6~1: Not used, set to "0" all the time.

Bit 0 (URSS): UART clock source select bit

0: Fc is set to Fs

1: Fc is set to Fm

6.1.34 Bank 2 RF

These are reserved registers.

6.1.35 Bank 3 R5

These are reserved registers.

6.1.36 Bank 3 R6: TBHP (Table Point Register for Instruction TBRD)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MLB	-	-	-	-	-	RBit9	RBit8

Bit 7 (MLB): Choosing MSB or LSB machine code to be moved to the register. The machine code is pointed by TBLP and TBHP register.

Bits 6 ~ 2: Not used, set to "**0**" all the time

Bits 1 ~ 0: These are the most two significant bits of address for program code.

6.1.37 Bank 3 R7: CMP2CON (Comparator 2 Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	CIS21	CIS20	CPOUT2	COS21	COS20	CPS21	CPS20

Bit 7: Not used, set to "**0**" all the time

Bit 6~5 (CIS21~CIS20): Inverting end 1 of Comparator 2 select bits.

CIS21	CIS20	Function Description
0	0	C2- is connected to P82
0	1	C2- is connected to P61
1	0	C2- is connected to P62
1	1	C2- is connected to P63

Bit 4 (CPOUT2): The result of Comparator 2 output.

Bit 3~2 (COS21~COS20): Comparator 2 Select bits.

COS21	COS20	Function Description
0	0	Comparator 2 is not used, P80 acts as normal I/O pin
0	1	Acts as a Comparator 2 and P80 acts as normal I/O pin
1	x	Acts as a Comparator 2 and P80 acts as Comparator 2 output pin (CO)

Bit 1~0 (CPS21~CPS20): Non-inverting end of Comparator 2 select bits.

CPS21	CPS20	Function Description
0	0	C2+ is connected to P81
0	1	C2+ is connected to ADC Internal Reference Voltage*
1	x	C2+ is connected to 1/2 VDD

***:** Select 2.048V/2.560V/3.072V/4.096V by control bit IRVS1~0 (Bank 2 R7) when ICTS is 1.

6.1.38 Bank 3 R8 ~ RC

These are reserved registers.

6.1.39 Bank 3 RD: TC3CR (Timer 3 Control)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC3FF1	TC3FF0	TC3S	TC3CK2	TC3CK1	TC3CK0	TC3M1	TC3M0

Bits 7 ~ 6 (TC3FF1 ~ TC3FF0): Timer/Counter 3 flip-flop control

TC3FF1	TC3FF0	Operating Mode
0	0	Clear
0	1	Toggle
1	0	Set
1	1	Reserved

Bit 5 (TC3S): Timer/Counter 3 start control

0: Stop and clear the counter

1: Start

Bits 4 ~ 2 (TC3CK2 ~ TC3CK0): Timer/Counter 3 clock source select

TC3CK2	TC3CK1	TC3CK0	Clock Source	Resolution	Max. Time	Resolution	Max. Time
			Normal, Idle	Fc=4M	Fc=4M	Fc=16K	Fc=16K
0	0	0	$Fc/2^{11}$	512 µs	131072 µs	128 ms	32768 ms
0	0	1	$Fc/2^{7}$	32 µs	8192 µs	8 ms	2048 ms
0	1	0	$Fc/2^{5}$	8 µs	2048 µs	2 ms	512 ms
0	1	1	$Fc/2^{3}$	2 µs	512 µs	500 µs	128 ms
1	0	0	$Fc/2^{2}$	1 µs	256 µs	250 µs	64 ms
1	0	1	$Fc/2^{1}$	500 ns	128 µs	125 µs	32 ms
1	1	0	Fc	250 ns	64 µs	62.5 µs	16 ms
1	1	1	External clock (TC3 pin)	-	-	-	-

Bits 1 ~ 0 (TC3M1 ~ TC3M0): Timer/Counter 3 operating mode select

TC3M1	TC3M0	Operating Mode
0	0	Timer/Counter
0	1	Reserved
1	0	Programmable Divider Output
1	1	Pulse Width Modulation Output

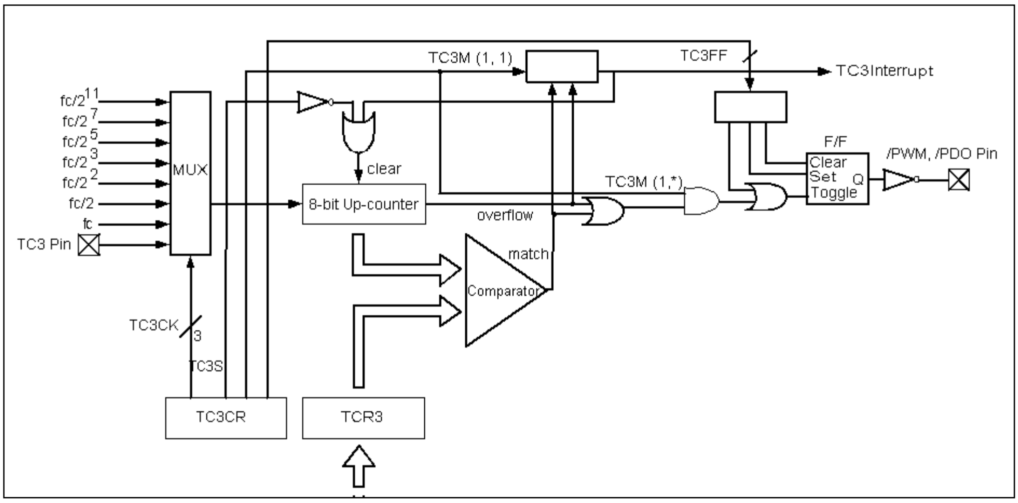


Figure 6-4 Timer / Counter 3 Configuration

In Timer mode, counting up is performed using the internal clock (rising edge trigger). When the contents of the up-counter match the TCR3, then interrupt is generated and the counter is cleared. Counting up resumes after the counter is cleared.

In Counter mode, counting up is performed using the external clock input pin (TC3 pin). When the contents of the up-counter match the TCR3, then interrupt is generated and the counter is cleared. Counting up resumes after the counter is cleared.

In Programmable Divider Output (PDO) mode, counting up is performed using the internal clock. The contents of TCR3 are compared with the contents of the up-counter. The F/F output is toggled and the counter is cleared each time a match is found. The F/F output is inverted and output to /PDO pin. This mode can generate 50% duty pulse output. **The F/F can be initialized by the program and it is initialized to "0" during reset**. A TC3 interrupt is generated each time a /PDO output is toggled.

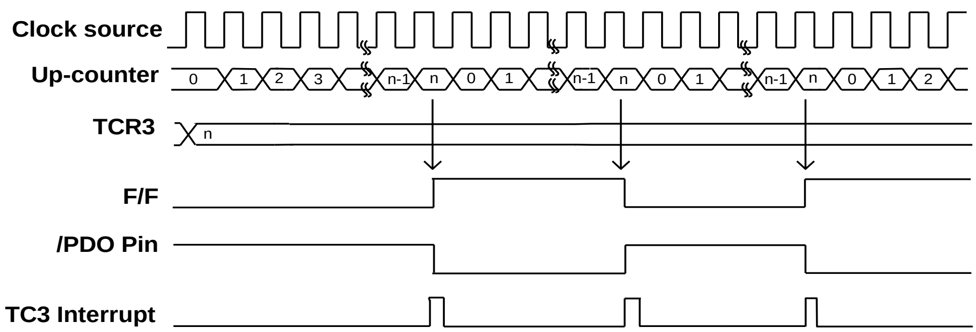


Figure 6-5 PDO Mode Timing Chart

In Pulse Width Modulation (PWM) Output Mode, counting up is performed using the internal clock. The contents of TCR3 are compared with the contents of the up-counter. The F/F is toggled when a match is found. The counter continues counting, the F/F is toggled again when the counter overflows, after which the counter is cleared. The F/F output is inverted and output to /PWM pin. A TC3 interrupt is generated each time an overflow occurs. **TCR3 is configured as a 2-stage shift register and, during output, will not switch until one output cycle is completed even if TCR3 is overwritten.** Therefore, the output can be changed continuously. Also, the first time, TCR3 is shifted by setting TC3S to "**1**" after data is loaded to TCR3.

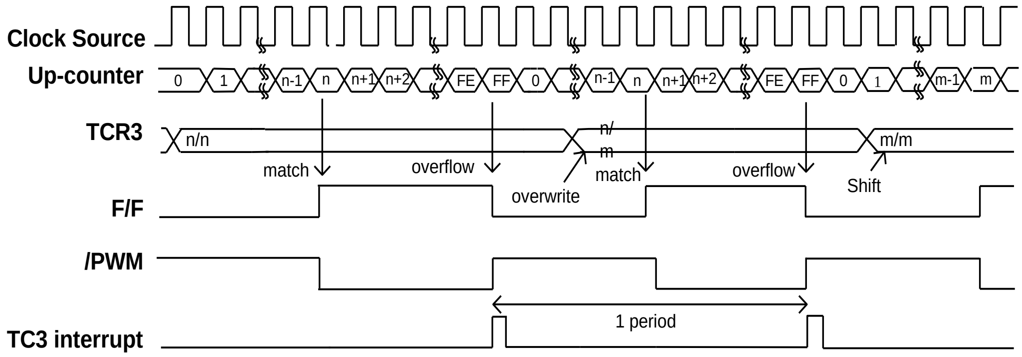


Figure 6-6 PWM Mode Timing Chart

6.1.40 Bank 3 RE: TC3D (Timer 3 Data Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC3D7	TC3D6	TC3D5	TC3D4	TC3D3	TC3D2	TC3D1	TC3D0

Bits 7 ~ 0 (TC3D7 ~ TC3D0): Data Buffer of 8-bit Timer/Counter 3

6.1.41 Bank 3 RF

These are reserved registers.

6.2 Special Function Registers

6.2.1 A (Accumulator)

Internal data transfer operation, or instruction operand holding usually involves the temporary storage function of the Accumulator. The Accumulator is not an addressable register.

6.2.2 CONT (Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTE	/INT	-	-	PSTE	PST2	PST1	PST0

Bit 7 (INTE): INT signal edge

0: Interrupt occurs at a rising edge of the INT pin

1: Interrupt occurs at a falling edge of the INT pin

Bit 6 (/INT): Interrupt Enable flag

0: Masked by DISI or hardware interrupt

1: Enabled by ENI/RETI instructions

Bits 5 ~ 4: Not used, set to “**0**” all the time

Bit 3 (PSTE): Prescaler enable bit for TCC

0: Prescaler disable bit, TCC rate is 1:1

1: Prescaler enable bit, TCC rate is set at Bit 2 ~ Bit 0.

Bit 2 ~ Bit 0 (PST 2 ~ PST0): TCC prescaler bits

PST2	PST1	PST0	TCC Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

The CONT register is both readable and writable.

6.2.3 IOC5 ~ IOC6, IOC8 (I/O Port Control Register)

A value of "**1**" sets the relative I/O pin into high impedance, while "**0**" defines the relative I/O pin as output.

IOC5 ~ IOC6, IOC8 registers are both readable and writable.

6.2.4 IOC7, IOC9

Reserved registers

6.2.5 IOCA: WDTCR (WDT Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTE	EIS	-	-	PSWE	PSW2	PSW1	PSW0

Bit 7 (WDTE): Control bit used to enable the Watchdog timer

0: Disable WDT

1: Enable WDT

WDTE is both readable and writable.

Bit 6 (EIS): Control bit used to define the function of P60 (/INT) pin

0: P60, bidirectional I/O pin

1: /INT, external interrupt pin. In this case, the I/O control bit of P60 (Bit 0 of IOC6) must be set to "**1**".

When EIS is "**0**", the path of /INT is masked. When EIS is "**1**", the status of the /INT pin can also be read by reading Port 6 (R6).

The EIS is both readable and writable.

Bits 5 ~ 4: Not used, set to "**0**" all the time

Bit 3 (PSWE): Prescaler enable bit for WDT

0: prescaler disable bit, WDT rate is 1:1

1: prescaler enable bit, WDT rate is set at Bit 0~Bit 2

Bit 2 ~ Bit 0 (PSW2 ~ PSW0): WDT prescaler bits

PSW2	PSW1	PSW0	WDT Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.2.6 IOCB: P6PDCR (Pull-down Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PD63	/PD62	/PD61	/PD60	-	-	-	/PD50

The IOCB Register is both readable and writable.

Bit 7 (/PD63): Control bit used to enable pull-down of the P63 pin.

0: Enable internal pull-down

1: Disable internal pull-down

Bit 6 (/PD62): Control bit used to enable pull-down of the P62 pin.

Bit 5 (/PD61): Control bit used to enable pull-down of the P61 pin.

Bit 4 (/PD60): Control bit used to enable pull-down of the P60 pin.

Bits 3 ~ 1: Not used, set to "**0**" all the time

Bit 0 (/PD50): Control bit used to enable pull-down of the P50 pin.

6.2.7 IOCC: P6ODCR (Open-drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	OD65	OD64	OD63	OD62	OD61	OD60

The IOCC Register is both readable and writable.

Bits 7 ~ 6: Not used, set to "**0**" all the time

Bit 5 (OD65): Control bit used to enable open-drain output of the P65 pin

0: Disable open-drain output

1: Enable open-drain output

Bit 4 (OD64): Control bit used to enable open-drain output of the P64 pin

Bit 3 (OD63): Control bit used to enable open-drain output of the P63 pin

Bit 2 (OD62): Control bit used to enable open-drain output of the P62 pin

Bit 1 (OD61): Control bit used to enable open-drain output of the P61 pin

Bit 0 (OD60): Control bit used to enable open-drain output of the P60 pin

6.2.8 IOCD: P9PHCR (Pull-high Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	/PH65	/PH64	/PH63	/PH62	/PH61	/PH60

The IOCD Register is both readable and writable.

Bits 7 ~ 6: Not used, set to "**0**" all the time

Bit 5 (/PH65): Control bit used to enable pull-high of the P65 pin.

0: Enable internal pull-high

1: Disable internal pull-high

Bit 4 (/PH64): Control bit used to enable pull-high of the P64 pin.

Bit 3 (/PH63): Control bit used to enable pull-high of the P63 pin.

Bit 2 (/PH62): Control bit used to enable pull-high of the P62 pin.

Bit 1 (/PH61): Control bit used to enable pull-high of the P61 pin.

Bit 0 (/PH60): Control bit used to enable pull-high of the P60 pin.

6.2.9 IOCE: IMR2 (Interrupt Mask Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMP2IE	-	TC3IE	-	TM1IE	UERRIE	URIE	UTIE

Bit 7 (CMP2IE): CMP2IF interrupt enable bit.

0: Disable CMP2IF interrupt

1: Enable CMP2IF interrupt

When the Comparator 2 output status change is used to enter an interrupt vector or enter the next instruction, the CMP2IE bit must be set to “Enable“.

Bit 6: Not used, set to “**0**” all the time

Bit 5 (TC3IE): Interrupt enable bit

0: Disable TC3IF interrupt

1: Enable TC3IF interrupt

Bits 4: Not used, set to “**0**” all the time

Bit 3 (TM1IE): TM1DBSF/TM1DASF interrupt enable bit.

0: Disable TM1SF interrupt.

1: Enable TM1SF interrupt.

Bit 2 (UERRIE): UERRIF interrupt enable bit.

0: Disable UERRIF interrupt.

1: Enable UERRIF interrupt.

Bit 1 (URIE): URIF interrupt enable bit.

0: Disable URIF interrupt.

1: Enable URIF interrupt.

Bit 0 (UTIE): UTSF interrupt enable bit.

0: Disable UTIF interrupt.

1: Enable UTIF interrupt.

NOTE:
The IOCE register is both readable and writable.

6.2.10 IOCF: IMR1 (Interrupt Mask Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SHIE	ADIE	-	-	-	EXIE	ICIE	TCIE

Bit 7(SHIF): SHIF interrupt enable bit

0: Disable SHIF interrupt

1: Enable SHIF interrupt

Bit 6 (ADIE): ADIF interrupt enable bit

0: Disable ADIF interrupt

1: Enable ADIF interrupt

When ADC complete status is used to enter an interrupt vector or enter the next instruction, the ADIE bit must be set to "Enable".

Bits 5 ~ 3: Not used, set to "0" all the time

Bit 2 (EXIE): EXIF interrupt enable bit

0: Disable EXIF interrupt

1: Enable EXIF interrupt

Bit 1 (ICIE): ICIF interrupt enable bit

0: Disable ICIF interrupt

1: Enable ICIF interrupt

Bit 0 (TCIE): TCIF interrupt enable bit

0: Disable TCIF interrupt

1: Enable TCIF interrupt

NOTES:

1. *User must set Bit 7 of the IOCF register to "**0**".*
2. *Individual interrupt is enabled by setting its associated control bit in the IOCF to "**1**".*
3. *Global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction.*
4. *The IOCF register is both readable and writable.*

6.3 TCC/WDT and Prescaler

There are two 8-bit counters available as prescalers for the TCC and WDT respectively. The PST2~PST0 bits of the CONT register are used to determine the ratio of the prescaler of TCC. Likewise, the PSW2~PSW0 bits of the IOCA register are used to determine the WDT prescaler. The prescaler counter will be cleared by the instructions each time they are written into TCC. The WDT and prescaler will be cleared by the "WDTC" and "SLEP" instructions. Figure 6.7 below depicts the EM78F811N circuit diagram of TCC/WDT.

R1 (TCC) is an 8-bit timer. The TCC clock source can only be an internal clock. When the TCC signal sourced from an internal clock, TCC will be incremented by 1 at Fc clock (without prescaler). **The TCC will stop running when sleep mode occurs**.

The watchdog timer is a free running on-chip RC oscillator. The WDT will keep on running even after the oscillator driver has been turned off (i.e. in sleep mode). During normal operation or sleep mode, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled any time during normal mode by software programming. Refer to the WDTE bit of the IOCA register. With no prescaler, the WDT time-out period is approximately 16 ms (one oscillator start-up timer period).

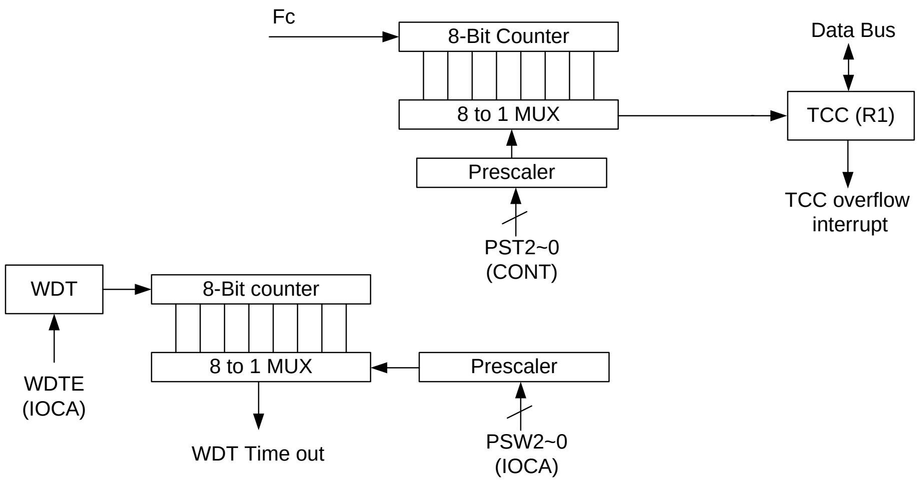
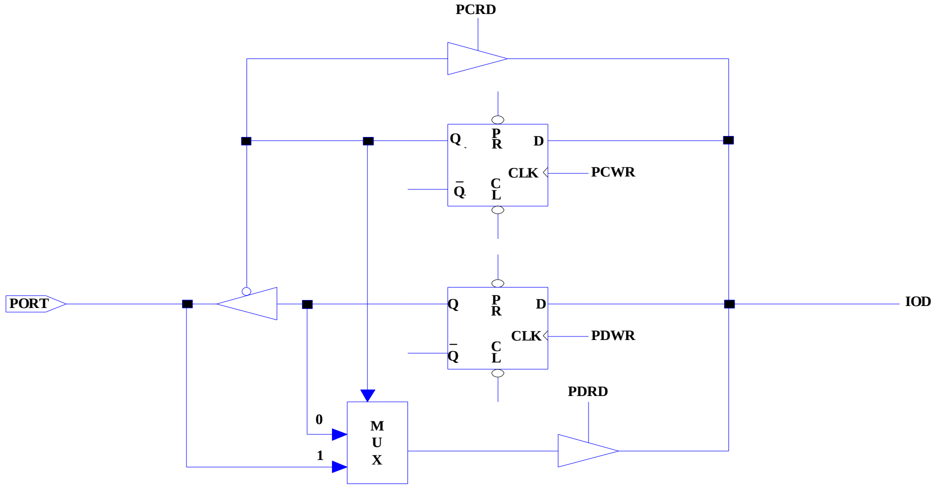


Figure 6.7 Block Diagram of TCC and WDT

6.4 I/O Ports

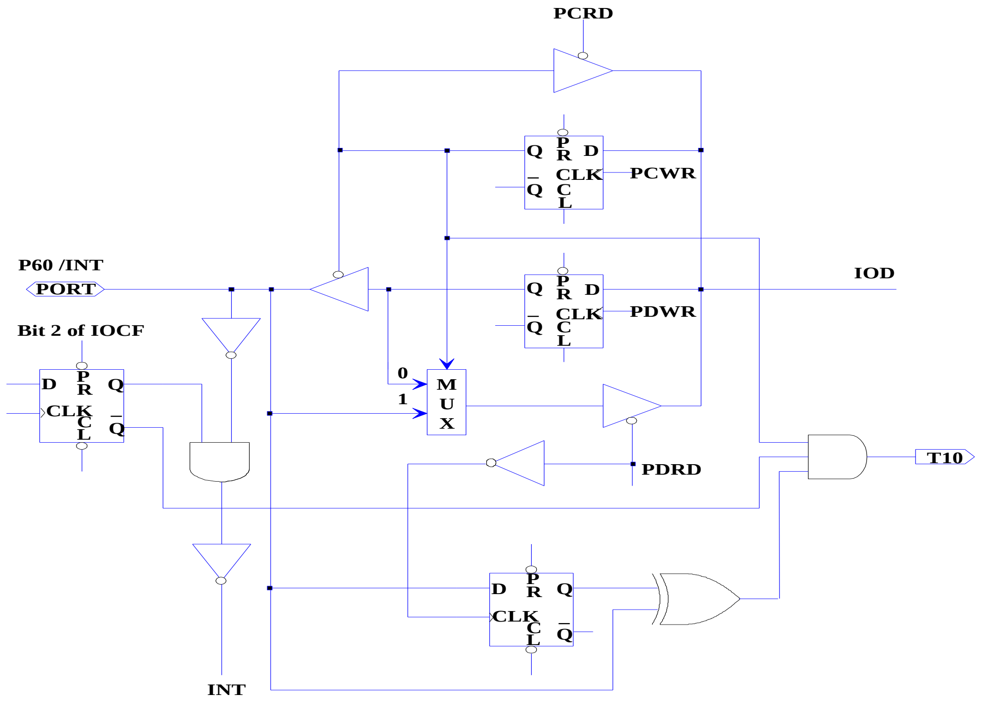
The I/O registers, Ports 5, 6 and 8, are bidirectional tri-state I/O ports. Port 6 can be pulled-high internally by software. In addition, Port 6 can also have open-drain output by software. Input status change interrupt (or wake-up) function on Port 6, P50, P60 ~ P63 pins can be pulled down by software. Each I/O pin can be defined as "input" or "output" pin by the I/O control register (IOC5 ~ IOC6, IOC8).

The I/O registers and I/O control registers are both readable and writable. The I/O interface circuits for Ports 5 ~ 6 and Port 8 are shown in the following Figures 6-8, 6-9(a), 6-9(b), and Figure 6-10.



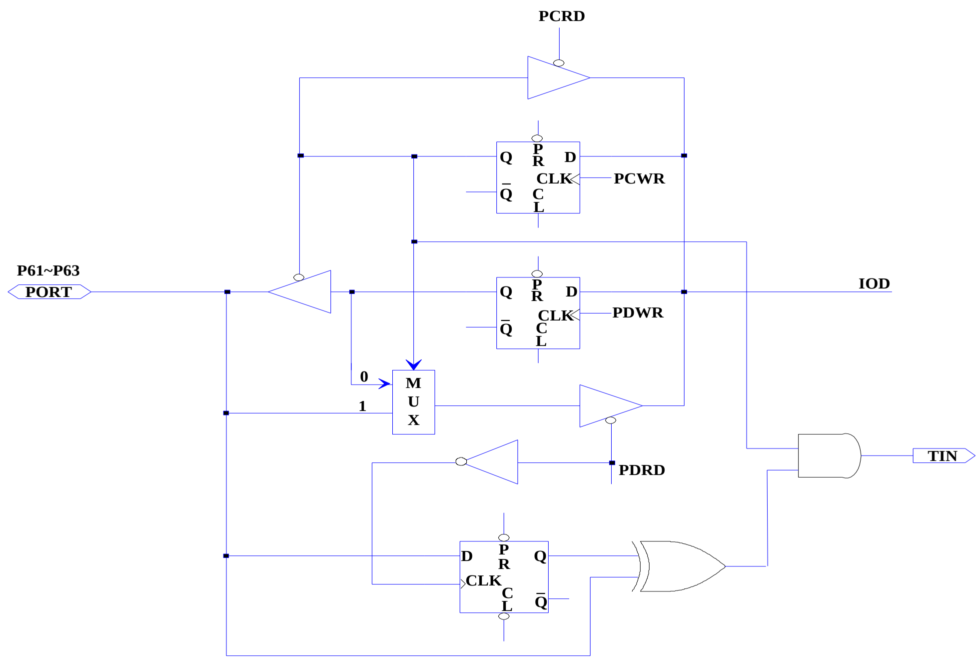
NOTE:
Pull-down is not shown in the figure.

Figure 6-8 Circuit of I/O Port and I/O Control Register for Ports 5 ~ 6, Port 8



NOTE: Pull-high (down) and Open-drain are not shown in the figure.

Figure 6-9(a) Circuit of I/O Port and I/O Control Register for P60 (/INT)



Note: Pull-high (down) and Open-drain are not shown in the figure.

Figure 6-9(b) Circuit of I/O Port and I/O Control Register for P61~P65

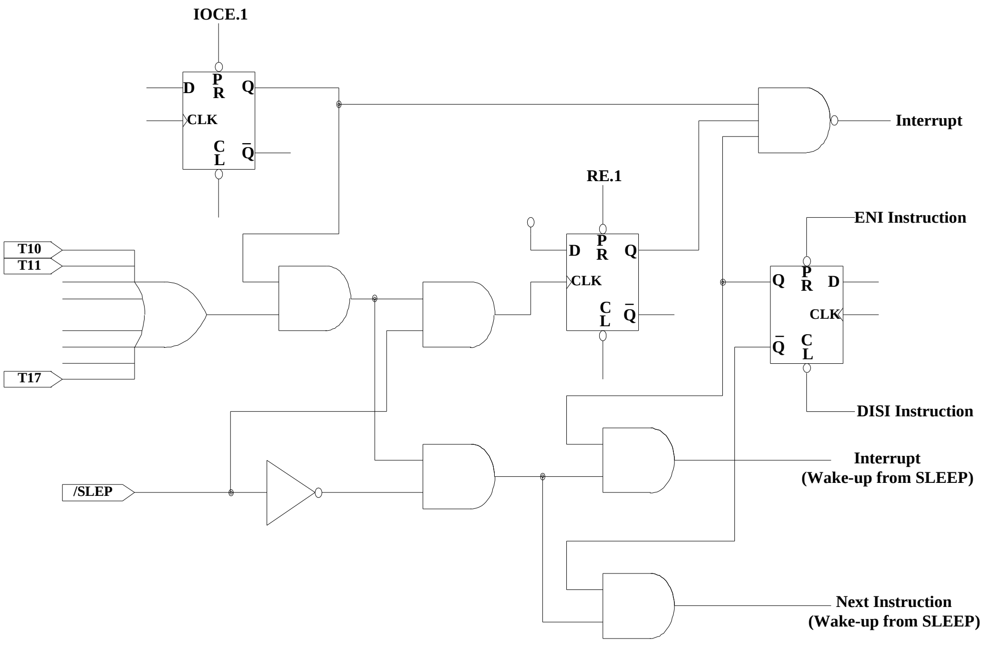


Figure 6-10   Block Diagram of I/O Port 6 with Input Change Interrupt/Wake-up

6.4.1 Usage of Port 6 Input Change Wake-up/Interrupt Function

Usage of Port 6 Input Status Changed Wake-up/Interrupt	
(I) Wake-up from Port 6 Input Status Change	(II) Port 6 Input Status Change Interrupt
a) Before Sleep	1. Read I/O Port 6 (MOV R6,R6)
1. Disable WDT[2] (use this very carefully)	2. Execute "ENI"
2. Read I/O Port 6 (MOV R6,R6)	3. Enable interrupt (Set IOCF.1)
3a. Enable interrupt (Set IOCF.1) after wake-up if “ENI” switch to interrupt Vector (006H), or if “DISI” excute next instruction	4. IF Port 6 change (interrupt) → Interrupt Vector (006H)
3b. Disable interrupt (Set IOCF.1), always execute next instruction	
4. Enable wake-up enable bit (Set RA.6)	
5. Execute "SLEP" instruction	
b) After Wake-up	
1. IF "ENI" → Interrupt Vector (006H)	
2. IF "DISI" → Next instruction	

[2] *The Software disables the WDT (Watchdog Timer) but the hardware must be enabled before applying Port 6 Change wake-up function. (Code Option Register and Bit 6 (ENWDTB) are set to “**1**”).*

6.5 Reset and Wake-up

6.5.1 Reset

A reset is initiated by one of the following events**:**

1) Power-on reset
2) /RESET pin input "low"
3) WDT time-out (if enabled)

The device is kept in a reset condition for a period of approximately 18ms(one oscillator start-up timer period) after a reset is detected.

- The oscillator is running, or will be started.
- The Program Counter (R2) is set to all "**0**".
- All I/O port pins are configured as input mode (high-impedance state).
- The Watchdog timer and prescaler are cleared.
- When power is switched on, the upper three bits of R3 are cleared.
- The bits of the RB, RC, RD registers are set to their previous status.
- The bits of the CONT register are set to all "**0**".
- The bits of the IOCA register are set to all "**0**".
- The bits of the IOCB register are set to all "**1**".
- The bits of the IOCC register are set to all "**0**".
- The bits of the IOCD register are set to all "**1**".
- The bits of the IOCE register are set to all "**0**".
- The bits of the IOCF register are set to all "**0**".

Sleep (power down) mode is asserted by executing the "SLEP" instruction. While entering Sleep mode, the WDT (if enabled) is cleared but keeps on running. After a wake-up, the wake-up time is 10µs for RC mode and is 800 µs for High Crystal mode.

The controller can be awakened by**:**

1) External reset input on /RESET pin
2) WDT time-out (if enabled)
3) Port 6 input status changes (if enabled)
4) Comparator output status changed (if CMPWE is enabled).
5) Completion of AD conversion (if ADWE is enabled).
6) External (P60, /INT) pin changes (if EXWE is enabled).

The first two cases (Case 1 and Case 2) will cause the EM78F811N to reset. The T and P flags of R3 can be used to determine the source of the reset (wake-up). Cases 3, 4, 5, 6 are considered the continuation of program execution and the global interrupt ("ENI" or "DISI" being executed) determines whether or not the controller branches to the interrupt vector following a wake-up. If ENI is executed before SLEP, the instruction will begin to execute from the Address 0×6, 0×15, 0×30, 0×3 after wake-up. If DISI is executed before SLEP, the execution will restart from the instruction right next to SLEP after wake-up. After a wake-up, the RC mode wake-up time is 10µs and the High Crystal mode wake-up time is 800µs.

One or more of Cases 2 to 6 can be enabled before entering into Sleep mode. That is-

a) If WDT is enabled before SLEP, all of the RE bits are disabled. Hence, the EM78F811N can be awakened only by Case 1 or 2. Refer to section on Interrupt (Section 6.6) for further details.

b) If Port 6 Input Status Change is used to wake-up EM78F811N and ICWE bit of RA register is enabled before SLEP, the WDT must be disabled. Hence, the EM78F811N can wake-up only by Case 3.

c) If Comparator 2 output status change is used to wake-up EM78F811N and CMPWE bit of RA register is enabled before SLEP, WDT must be disabled by software. Hence, the EM78F811N can wake-up only by Case 4.

d) If AD conversion completed is used to wake-up EM78F811N and ADWE bit of RA register is enabled before SLEP, the WDT must be disabled by software. Hence, the EM78F811N can wake-up only by Case 5.

e) If External (P60,/INT) pin change is used to wake-up EM78F811N and EXWE bit of RA register is enabled before SLEP, the WDT must be disabled. Hence, the EM78F811N can wake-up only by Case 6.

If Port 6 Input Status Change Interrupt is used to wake-up the EM78F811N, (as in Case [b] above), the following instructions must be executed before SLEP**:**

```
MOV             A, @0xxx1000b  ; Select WDT prescaler and
                               ; Disable the WDT
IOW             IOCA
WDTC                           ; Clear WDT and prescaler
MOV             R6, R6         ; Read Port 6
ENI  (or DISI)                 ; Enable (or disable) global
                               ; interrupt
BC              R4, 7          ; Select Bank0
BC              R4, 6
MOV             A, @0100xxxxb  ; Enable Port 6 input change
                               ; wake-up bit
MOV             RA,A
MOV             A, @xxxxxx1xb  ; Enable Port 6 input change
                               ; interrupt
IOW             IOCF
SLEP                           ; Sleep
```

Similarly, if the Comparator 2 Interrupt is used to wake up the EM78F811N (as in Case [c] above), the following instructions must be executed before SLEP:

```
BS              R4, 7          ; Select Bank 3
BS              R4, 6
MOV             A, @xxxx10xxb  ; Select a comparator and P80 act
                               ; as CO pin
MOV             R7,A
MOV             A, @0xxx1000b  ; Select WDT prescaler and
                               ; Disable the WDT
IOW             IOCA
WDTC                           ; Clear WDT and prescaler
ENI (or DISI)                  ; Enable (or disable) global
                               ; interrupt
BC              R4, 7          ; Select Bank 0
BC              R4, 6
MOV             A, @1000xxxxb  ; Enable comparator output status
                               ; change wake-up bit
MOV             RA,A
MOV             A, @10000000b  ; Enable comparator output status
                               ; change interrupt
IOW             IOCE
SLEP                           ; Sleep
```

6.5.2 Summary of Wake-up and Interrupt Modes Operation

<table>
<tr><th rowspan="2">Wake-up Signal</th><th rowspan="2">Condition Signal</th><th colspan="2">Sleep Mode</th><th colspan="2">Idle Mode</th><th colspan="2">Green Mode</th><th colspan="2">Normal Mode</th></tr>
<tr><th>DISI</th><th>ENI</th><th>DISI</th><th>ENI</th><th>DISI</th><th>ENI</th><th>DISI</th><th>ENI</th></tr>
<tr><td rowspan="4">External INT</td><td>EXWE = 0, EXIE = 0</td><td colspan="2">Wake-up is invalid</td><td colspan="2">Wake-up is invalid</td><td colspan="2">Interrupt is invalid</td><td colspan="2">Interrupt is invalid</td></tr>
<tr><td>EXWE = 0, EXIE = 1</td><td colspan="2">Wake-up is invalid</td><td colspan="2">Wake-up is invalid</td><td>Next Instruction</td><td>Interrupt + Interrupt Vector</td><td>Next Instruction</td><td>Interrupt + Interrupt Vector</td></tr>
<tr><td>EXWE = 1, EXIE = 0</td><td colspan="2">Wake up + Next Instruction</td><td colspan="2">Wake up + Next Instruction</td><td colspan="2">Interrupt is invalid.</td><td colspan="2">Interrupt is invalid</td></tr>
<tr><td>EXWE = 1, EXIE = 1</td><td>Wake up + Next Instruction</td><td>Wake up + Interrupt Vector</td><td>Wake up + Next Instruction</td><td>Wake up + Interrupt Vector</td><td>Next Instruction</td><td>Interrupt + Interrupt Vector</td><td>Next Instruction</td><td>Interrupt + Interrupt Vector</td></tr>
<tr><td rowspan="4">Port 6 pin change</td><td>ICWE = 0, ICIE = 0</td><td colspan="2">Wake-up is invalid</td><td colspan="2">Wake-up is invalid</td><td colspan="2">Interrupt is invalid</td><td colspan="2">Interrupt is invalid</td></tr>
<tr><td>ICWE = 0, ICIE = 1</td><td colspan="2">Wake-up is invalid</td><td colspan="2">Wake-up is invalid</td><td>Next Instruction</td><td>Interrupt + Interrupt Vector</td><td>Next Instruction</td><td>Interrupt + Interrupt Vector</td></tr>
<tr><td>ICWE = 1, ICIE = 0</td><td colspan="2">Wake up + Next Instruction</td><td colspan="2">Wake up + Next Instruction</td><td colspan="2">Interrupt is invalid</td><td colspan="2">Interrupt is invalid</td></tr>
<tr><td>ICWE = 1, ICIE = 1</td><td>Wake up + Next Instruction</td><td>Wake up + Interrupt Vector</td><td>Wake up + Next Instruction</td><td>Wake up + Interrupt Vector</td><td>Next Instruction</td><td>Interrupt + Interrupt Vector</td><td>Next Instruction</td><td>Interrupt + Interrupt Vector</td></tr>
<tr><td rowspan="2">TCC overflow</td><td>TCIE = 0</td><td colspan="2">Wake-up is invalid</td><td colspan="2">Wake-up is invalid</td><td colspan="2">Interrupt is invalid</td><td colspan="2">Interrupt is invalid</td></tr>
<tr><td>TCIE = 1</td><td colspan="2">Wake-up is invalid</td><td>Wake up + Next Instruction</td><td>Wake up + Interrupt Vector</td><td>Next Instruction</td><td>Interrupt + Interrupt Vector</td><td>Next Instruction</td><td>Interrupt + Interrupt Vector</td></tr>
<tr><td rowspan="4">Comparator 2 (Comparator Output Status Change)</td><td>CMP2WE = 0, CMP2IE = 0</td><td colspan="2">Wake-up is invalid</td><td colspan="2">Wake-up is invalid</td><td colspan="2">Interrupt is invalid</td><td colspan="2">Interrupt is invalid</td></tr>
<tr><td>CMP2WE = 0, CMP2IE = 1</td><td colspan="2">Wake-up is invalid</td><td colspan="2">Wake-up is invalid</td><td>Next Instruction</td><td>Interrupt + Interrupt Vector</td><td>Next Instruction</td><td>Interrupt + Interrupt Vector</td></tr>
<tr><td>CMP2WE = 1, CMP2IE = 0</td><td colspan="2">Wake up + Next Instruction</td><td colspan="2">Wake up + Next Instruction</td><td colspan="2">Interrupt is invalid</td><td colspan="2">Interrupt is invalid</td></tr>
<tr><td>CMP2WE = 1, CMP2IE = 1</td><td>Wake up + Next Instruction</td><td>Wake up + Interrupt Vector</td><td>Wake up + Next Instruction</td><td>Wake up + Interrupt Vector</td><td>Next Instruction</td><td>Interrupt + Interrupt Vector</td><td>Next Instruction</td><td>Interrupt + Interrupt Vector</td></tr>
</table>

(Continuation)

Wake-up Signal	Condition Signal	Sleep Mode		Idle Mode		Green Mode		Normal Mode	
		DISI	ENI	DISI	ENI	DISI	ENI	DISI	ENI
TM1 overflow	TMIE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	TMIE = 1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
UART Transmit complete Interrupt	URWK = 0, UTIE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	URWK = 0, UTIE = 1	Wake-up is invalid		Wake-up is invalid		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	URWK = 1*, UTIE = 0	Wake-up is invalid		Wake up + Next Instruction	Wake up + Next Instruction	Interrupt is invalid		Interrupt is invalid	
	URWK = 1*, UTIE = 1	Wake-up is invalid		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
UART Receive data Buffer full Interrupt	URWK = 0, URIE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	URWK = 0, URIE = 1	Wake-up is invalid		Wake-up is invalid		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	URWK = 1*, URIE = 0	Wake-up is invalid		Wake up + Next Instruction	Wake up + Next Instruction	Interrupt is invalid		Interrupt is invalid	
	URWK = 1*, URIE = 1	Wake-up is invalid		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
UART Receive Error Interrupt	URWK = 0, UERRIE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	URWK = 0, UERRIE = 1	Wake-up is invalid		Wake-up is invalid		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	URWK = 1*, UERRIE = 0	Wake-up is invalid		Wake up + Next Instruction	Wake up + Next Instruction	Interrupt is invalid		Interrupt is invalid	
	URWK = 1*, UERRIE = 1	Wake-up is invalid		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector

(Continuation)

Wake-up Signal	Condition Signal	Sleep Mode		Idle Mode		Green Mode		Normal Mode	
		DISI	ENI	DISI	ENI	DISI	ENI	DISI	ENI
TC3 interrupt	TC3IE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	TC3IE = 1	Wake-up is invalid		Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
AD Conversion Complete Interrupt	ADWE = 0, ADIE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	ADWE = 0, ADIE = 1	Wake-up is invalid		Wake-up is invalid		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	ADWE = 1*, ADIE = 0	Wake up + Next Instruction		Wake up + Next Instruction		Interrupt is invalid		Interrupt is invalid	
	ADWE = 1*, ADIE = 1	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector

* Fs and Fm don't stop.

6.5.3 Summary of Registers Initialized Values

Legend: **x:** *Not used* **P:** *Previous value before reset*
u: *Unknown or don't care* **t:** *Refer to the tables under Section 6.5.4*

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N/A	IOC5	Bit Name	C57	-	C55	C54	-	-	-	C50
		Power-on	1	0	1	1	0	0	0	1
		/RESET and WDT	1	0	1	1	0	0	0	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC6	Bit Name	-	-	C65	C64	C63	C62	C61	C60
		Power-on	0	0	1	1	1	1	1	1
		/RESET and WDT	0	0	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC8	Bit Name	-	-	-	-	C83	C82	C81	C80
		Power-on	0	0	0	0	1	1	1	1
		/RESET and WDT	0	0	0	0	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	CONT	Bit Name	INTE	INT	-	-	PSTE	PST2	PST1	PST0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

(Continuation)

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0×00	R0 (IAR)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×01	R1 (TCC)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×02	R2 (PC)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	Jump to interrupt vector address or continue to execute next instruction							
0×03	R3 (SR)	Bit Name	-	-	-	T	P	Z	DC	C
		Power-on	0	0	0	1	1	U	U	U
		/RESET and WDT	0	0	0	t	t	P	P	P
		Wake-up from Pin Change	P	P	P	t	t	P	P	P
0×04	R4 (RSR)	Bit Name	Bank 1	Bank 0	-	-	-	-	-	-
		Power-on	0	0	1	U	U	U	U	U
		/RESET and WDT	0	0	1	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×05	P5 (Bank 0)	Bit Name	P57	-	P55	P54	-	-	-	P50
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×06	P6 (Bank 0)	Bit Name	-	-	P65	P64	P63	P62	P61	P60
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×08	P8 (Bank 0)	Bit Name	-	-	-	-	P83	P82	P81	P80
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

(Continuation)

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0×09	R9 (Bank 0)	Bit Name	RBit7	RBit6	RBit5	RBit4	RBit3	RBit2	RBit1	RBit0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0A	RA (Bank 0)	Bit Name	CMP2WE	ICWE	ADWE	EXWE	URWE	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0B	RB (ECR) (Bank 0)	Bit Name	RD	WR	EEWE	EEDF	EEPC	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0C	RC (Bank 0)	Bit Name	-	EE_A6	EE_A5	EE_A4	EE_A3	EE_A2	EE_A1	EE_A0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0D	RD (Bank 0)	Bit Name	EE_D7	EE_D6	EE_D5	EE_D4	EE_D3	EE_D2	EE_D1	EE_D0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0E	RE (Bank 0)	Bit Name	PERCS	TIMERSC	CPUS	IDLE	-	-	-	-
		Power-on	0	1	1	1	0	0	0	0
		/RESET & WDT	0	1	1	1	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0F	RF (ISR) (Bank 0)	Bit Name	SHIF	ADIF	-	-	-	EXIF	ICIF	TCIF
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×08	R8 (Bank 1)	Bit Name	RCM1	RCM0	RCM2	-	-	-	-	-
		Power-on	Word 1<4,3,2>			0	0	0	0	0
		/RESET & WDT	Word 1<4,3,2>			0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

(Continuation)

Addr	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0×09	R9 (Bank 1)	Bit Name	TM1S	TM1RC	TM1SS1	TM1SS0	TM1FF	TM1MOS	TM1IS1	TM1IS0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0A	RA (Bank 1)	Bit Name	TM1M2	TM1M1	TM1M0	-	TM1CK3	TM1CK2	TM1CK1	TM1CK0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0B	RB (Bank 1)	Bit Name	TM1DAH7	TM1DAH6	TM1DAH5	TM1DAH4	TM1DAH3	TM1DAH2	TM1DAH1	TM1DAH0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0C	RC (Bank 1)	Bit Name	TM1DAL7	TM1DAL6	TM1DAL5	TM1DAL4	TM1DAL3	TM1DAL2	TM1DAL1	TM1DAL0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0D	RD (Bank 1)	Bit Name	TM1DBH7	TM1DBH6	TM1DBH5	TM1DBH4	TM1DBH3	TM1DBH2	TM1DBH1	TM1DBH0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0E	RE (Bank 1)	Bit Name	TM1DBL7	TM1DBL6	TM1DBL5	TM1DBL4	TM1DBL3	TM1DBL2	TM1DBL1	TM1DBL0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0F	RF (Bank 1)	Bit Name	CMP2IF	-	TC3IF	TM1DBSF	TM1DASF	UERRIF	URIF	UTIF
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×05	R5 (Bank 2)	Bit Name	-	-	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

(Continuation)

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0×06	R6 (Bank 2)	Bit Name	CKR2	CKR1	CKR0	ADRUN	ADPD	ADIS2	ADIS1	ADIS0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×07	R7 (Bank 2)	Bit Name	ADLPFEN	-	-	IRVS2	IRVS1	IRVS0	SHS1	SHS0
		Power-on	0	0	0	0	0	0	1	0
		/RESET and WDT	0	0	0	0	0	0	1	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×08	R8 (Bank 2)	Bit Name	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×09	R9 (Bank 2)	Bit Name	-	-	-	-	AD3	AD2	AD1	AD0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x0A	RA (Bank 2)	Bit Name	UINVEN	UMODE1	UMODE0	BRATE2	BRATE1	BRATE0	UTBF	TXE
		Power-on	0	0	0	0	0	0	1	0
		/RESET and WDT	0	0	0	0	0	0	1	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x0B	RB (Bank 2)	Bit Name	URTD8	EVEN	PRE	PRERR	OVERR	FMERR	URBF	RXE
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x0C	RC (Bank 2)	Bit Name	URTD7	URTD6	URTD5	URTD4	URTD3	URTD2	URTD1	URTD0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x0D	RD (Bank 2)	Bit Name	URRD7	URRD6	URRD5	URRD4	URRD3	URRD2	URRD1	URRD0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x0E	RE (Bank 2)	Bit Name	URRD8	-	-	-	-	-	-	URSS
		Power-on	0	0	0	0	0	0	0	1
		/RESET and WDT	0	0	0	0	0	0	0	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

(Continuation)

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0×06	R6 (Bank 3)	Bit Name	MLB	-	-	-	-	-	RBit9	RBit8
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×07	R7 (Bank 3)	Bit Name	-	-	-	CPOUT2	COS21	COS20	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×08	R8 (Bank 3)	Bit Name	-	CIS21	CIS20	CPOUT2	COS21	COS20	CPS21	CPS20
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0D	RD (Bank 3)	Bit Name	TC3FF1	TC3FF0	TC3S	TC3CK2	TC3CK1	TC3CK0	TC3M1	TC3M0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0E	RE (Bank 3)	Bit Name	TC3D7	TC3D6	TC3D5	TC3D4	TC3D3	TC3D2	TC3D1	TC3D0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

(Continuation)

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0×0A	IOCA	Bit Name	WDTE	EIS	-	-	PSWE	PSW2	PSW1	PSW0
		Power-un	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0B	IOCB	Bit Name	/PD63	/PD62	/PD61	/PD60	-	-	-	/PD50
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0C	IOCC	Bit Name	-	-	OD65	OD64	OD63	OD62	OD61	OD60
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0D	IOCD	Bit Name	-	-	/PH65	/PH64	/PH63	/PH62	/PH61	/PH60
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0E	IOCE	Bit Name	CMP2IE	-	TC3IE	-	TM1IE	UERRIE	URIE	UTIE
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0F	IOCF	Bit Name	SHIE	ADIE	-	-	-	EXIE	ICIE	TCIE
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×10 ~ 0×3F	R10~R3F	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

6.5.4 *Status of T and P of the Status Register*

A reset condition is initiated by following events**:**

1) Power-on condition

2) High-low-high pulse on /RESET pin

3) Watchdog timer time-out

The values of **T** and **P** in the following tables are used to check how the processor wakes up and shows the events that may affect the status of **T** and **P,** respectively.

■ **Values of T and P after Reset**

Reset Type	T	P
Power on	1	1
/RESET during operation mode	*P	*P
/RESET wake-up during Sleep mode	1	0
WDT during operation mode	0	*P
WDT wake-up during Sleep mode	0	0

* ***P:*** *Previous status before reset*

■ **Status of T and P Being Affected by Events**

Event	T	P
Power on	1	1
WDTC instruction	1	1
WDT time-out	0	*P
SLEP instruction	1	0
Wake-up on pin change during Sleep mode	1	0

* ***P:*** *Previous status before reset*

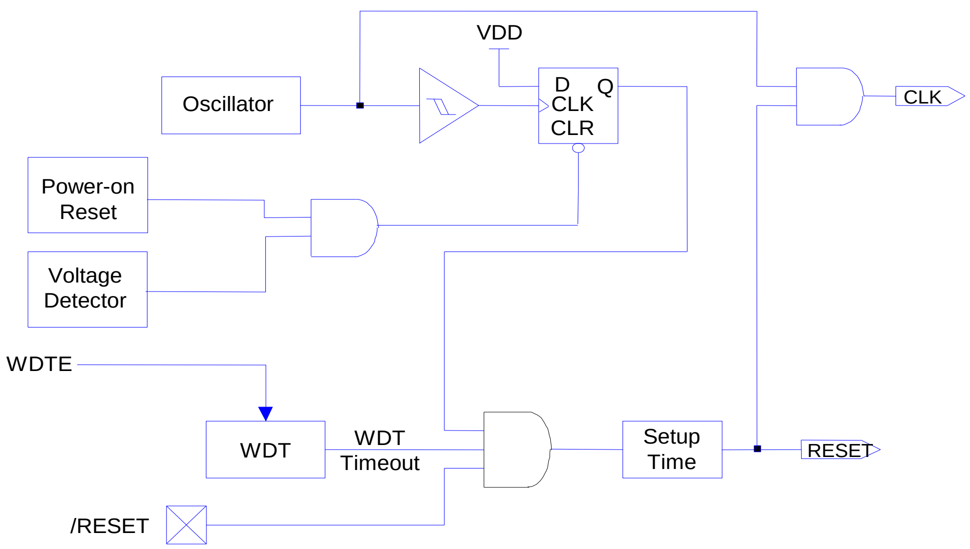


Figure 6-11 Block Diagram of Controller Reset

6.6 Interrupt

The EM78F811N has 11 interrupts (3 external, 8 internal) as listed below**:**

Interrupt Source		Enable Condition	Int. Flag	Int. Vector	Priority
Internal / External	Reset	-	-	0000	High 0
External	INT	ENI + EXIE=1	EXIF	0003	1
External	Port 6 pin change	ENI + ICIE=1	ICIF	0006	2
Internal	TCC	ENI + TCIE=1	TCIF	0009	3
Internal	System Hold	ENI + SHIE=1	SHIF	0012	4
External	Comparator 2	ENI + CMP2IE=1	CMP2IF	0015	5
Internal	TM1	ENI + TM1IE=1	TM1DASF TM1DBSF	0018	6
Internal	UART Rx error	ENI + UERRIE=1	UERRIF	001B	7
Internal	UART receive	ENI + URIE=1	URIF	001E	8
Internal	UART transimt	ENI + UTIE=1	UTIF	0021	9
Internal	TC3	ENI + TC3IE=1	TC3IF	0027	10
Internal	ADC	ENI + ADIE=1	ADIF	0030	11

RE and RF are the interrupt status registers that record the interrupt requests in the relative flags/bits. IOCE and IOCF are the interrupt mask registers. The global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. When one of the enabled interrupts occurs, the next instruction will be fetched from their individual address. The interrupt flag bit must be cleared by instructions before leaving the interrupt service routine and before interrupts are enabled to avoid recursive interrupts.

The flag (except ICIF bit) in the Interrupt Status Register (RF and RE) is set regardless of the status of its mask bit or the execution of ENI. The RETI instruction ends the interrupt routine and enables the global interrupt (the execution of ENI).

The external interrupt has an on-chip digital noise rejection circuit (input pulse less than **8 system clock time** is eliminated as noise), **but in Low Crystal oscillator (LXT) mode, the noise rejection circuit will be disabled**. When an interrupt (Falling edge) is generated by the External interrupt (when enabled), the next instruction will be fetched from Address 003H.

Before the interrupt subroutine is executed, the contents of ACC and the R3 and R4 register are saved by hardware. If another interrupt occurred, the ACC, R3 and R4 will be replaced by the new interrupt. After the interrupt service routine is completed, ACC,R3 and R4 are pushed back.

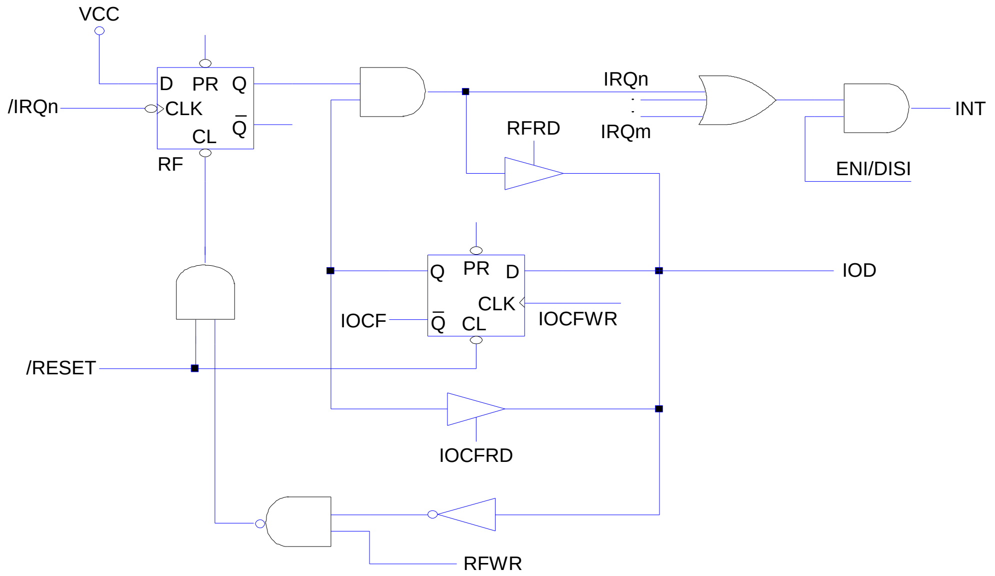


Figure 6-12 Interrupt Input Circuit

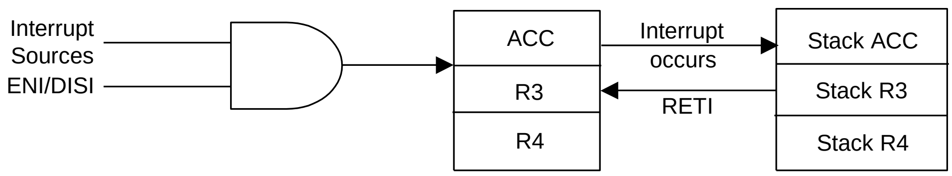


Figure 6-13 Interrupt Back-up Diagram

6.7 Data EEPROM

The Data EEPROM is readable and writable during normal operation over the whole Vdd range, but only writable with Vdd above 2.2V. The operation for Data EEPROM is based on a single byte. A write operation makes an erase-then-write cycle to take place on the allocated byte.

The Data EEPROM memory provides high erase-and-write cycles. A byte write automatically erases the location and writes the new value.

6.7.1 Data EEPROM Control Register

The EEPROM Control Register 9 (Bank 0 RB: EECR) is the control register for configuring and initiating the control register status.

When accessing the EEPROM data memory, the EEPROM address register (Bank 0 RC: EEPA) holds the address to be accessed. In accordance with the operation, the EEPROM Data register (Bank 0 RD: EEPD) holds the data to be written, or the data read, at the address in RC.

6.7.2 Programming Steps / Example Demonstration

■ **Programming Steps**

Follow these steps to write or read data from the EEPROM:

1) Set the RB.EEPC bit to “**1**” to enable the EEPROM power.
2) Write the address to RC (128 bytes EEPROM address).
   a) Set the RB.EEWE bit to “**1**”, if the write function is employed.
   b) Write the 8-bit data value to be programmed in the RD (128 bytes EEPROM data)
   c) Set the RB.WR bit to “**1**”, then execute write function
   d) Set the RB.READ bit to “**1**”, after which, execute read function
3) a) Wait for the RB.WR to be cleared
   b) Wait for the RB.EEDF to be cleared
4) For the next conversion, repeat from Step 2 as required.
5) If you want to save power, make sure the EEPROM data is switched off by clearing the RB.EEPC.

■ **Example Demonstration Programs**

```
;Define the control register
;Write data to EEPROM
RC == 0x0C
RB == 0x0B
RD == 0x0D
Read == 0x07
WR == 0x06
EEWE == 0x05
EEDF == 0x04
EEPC == 0x03

BS  RB, EEPC    ; Set the EEPROM power on
MOV A,@0x0A
MOV RC,A        ; Assign the address from EEPROM
BS  RB, EEWE    ; Enable the EEPROM write function
MOV A,@0x55
MOV RD,A        ; Set the data for EEPROM
BS  RB,WR       ; Write value to EEPROM
JBC RB,EEDF     ; Check whether the EEPROM bit is complete or not
JMP $-1
```

6.8 Analog-to-Digital Converter (ADC)

The analog-to-digital circuitry consists of a 12-bit analog multiplexer, three control registers [AISR/R5 (Bank 2), ADCON/R6 (Bank 2), ADCON2/R7 (Bank 2), two data registers (ADDH, ADDL/R8, R9), and an ADC with 12-bit resolution. The functional block diagram of the ADC is shown in Figure 6-14 below. The analog reference voltage (Vref) and analog ground are connected to internal voltage reference or via separate input pins.

The ADC module utilizes successive approximation to convert the unknown analog signal into a digital value. The result is fed to the ADDH and ADDL. Input channels are selected by the analog input multiplexer via the ADCON register Bits ADIS2 ~ ADIS0.

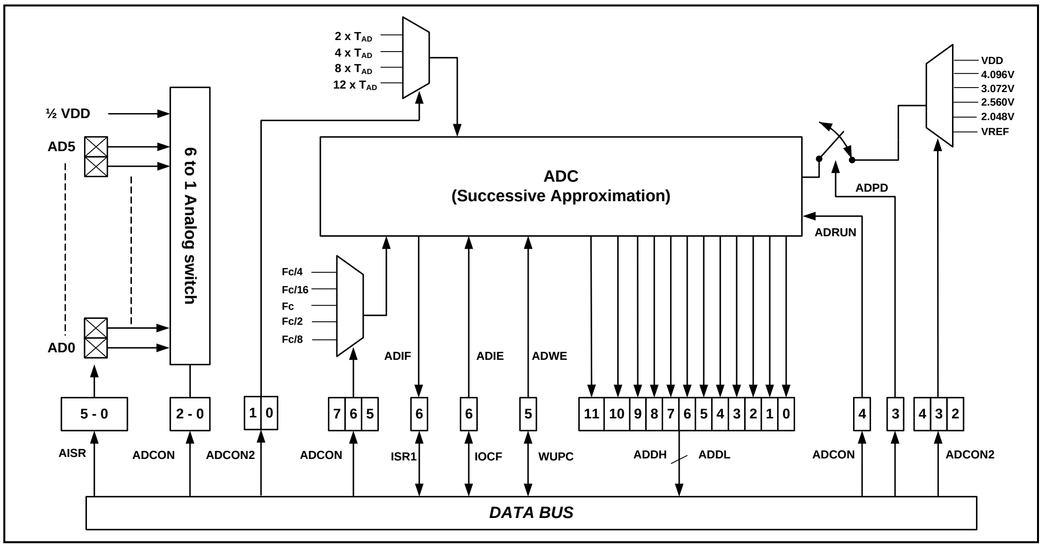


Figure 6-14 Functional Block Diagram of Analog-to-Digital Conversion

6.8.1 A/D Sampling Time

The accuracy, linearity, and speed of the successive approximation AD converter are dependent on the properties of the ADC and the comparator. The source impedance and the internal sampling impedance directly affect the time required to charge the sample holding capacitor. The application program controls the length of the sample time to meet the specified accuracy. Generally speaking, the program should wait for 2µs for each KΩ of the analog source impedance and at least 2µs for the low-impedance source. The maximum recommended impedance for analog source is 10KΩ at Vdd=5V. After the analog input channel is selected, this acquisition time must be done before the conversion can be started.

6.8.2 A/D Conversion Time

This allows the MCU to run at a maximum frequency without sacrificing the accuracy of AD conversion. The max ADC operation frequency is 2MHz. The ADC input clock is system clock divide by CKR2~0 and it must be less than of equal Max ADC Operating Frequency. The following table shows the relationship between ADC sampling time and the maximum ADC operating frequencies.

VDD	Max. ADC Clock Rate	Max. Conversion Time	Sample and Hold Timing Selection (SHS1~0)	Max. Conversion Rate
3.0V~5.5V	2MHz	0.5μs	8 x TAD	(12 + 8) x 0.5μs = 100KSPS
2.5V~3.0V	0.5MHz	2μs	8 x TAD	(12 + 8) x 2μs = 25KSPS

System Mode	CKR2~0	ADC Clock Rate	Max. system operation frequency in 2.5V~3.0V	Max. system operation frequency in 3.0V~5.5V
Normal Mode	000	Fm/4	2 MHz	8 MHz
	001	Fm/16	4 MHz	16 MHz
	010	Fm	0.5 MHz	2 MHz
	011	Fm/2	1 MHz	4 MHz
	1xx	Fm/8	4 MHz	16 MHz
Green Mode	000	Fs/4	Fs/4	Fs/4
	001	Fs/16	Fs/16	Fs/16
	010	Fs	Fs	Fs
	011	Fs/2	Fs/2	Fs/2
	1xx	Fs/8	Fs/8	Fs/8

NOTES:

1. *The pin that is not used as analog input can be used as regular input or output pin.*
2. *During conversion, do not perform output instruction in order to maintain precision for all the pins.*

6.8.3 A/D Operation during Sleep Mode

In order to obtain a more accurate ADC value and reduce power consumption, the AD conversion remains operational during Sleep mode. **As the SLEP instruction is executed, all MCU operations will stop except for the Oscillator, TCC, TC3, and AD conversion.**

The AD Conversion is considered completed when**:**

1 ADRUN bit of R6 register is cleared to “**0**”.

2 Wake-up from AD conversion remains in operation during Sleep Mode.

The result is fed to the ADDH, ADDL when the conversion is completed. If the ADWE is enabled, the device will wake up. Otherwise, the AD conversion will be shut off, no matter what the status of the ADPD bit is.

6.8.4 Programming Steps/Considerations

■ **Programming Steps**

Follow the following steps to obtain data from the ADC**:**

1. AD pins that are not data-converted must be set as high-impedance inputs and cannot be set as output pins (Pull-High or Pull-Low).
2. Write to the R6/ADCON register to configure the AD module:
   a) Define the AD conversion clock rate (CKR2 ~ CKR0).
   b) Select the Sampling and Hold time (SHS1 ~ SHS0).
   c) Select the VREFS input source of the ADC, wait at least 10us before set the ADLPFEN when ADC VREF is selected to internal source (IRVS2~IRVS0 = “001~100“).
   d) Set the ADPD bit to “**1**”, turn on ADC Power.
3. Select AD input channel (ADIS2 ~ ADIS0).
4. Enable the corresponding AD conversion pin (AISR) to the ADC input channel selected in Step 3.
5. Set the ADWE bit if the wake-up function is employed.
6. Set the ADIE bit if the interrupt function is employed.
7. Write “ENI” instruction if the interrupt function is employed.
8. Set the ADRUN bit to “**1**”.
9. Set a "SLEP" command or a loop check.
10. Wait for wake-up or for ADRUN bit to be cleared to “**0**”.
11. Read the ADDH and ADDL conversion data registers.
12. Clear the interrupt flag bit (ADIF) when AD interrupt function has occurred.
13. Turn off the selected AD conversion pin function (AISR).
14. For the next conversion, repeat from Step 3 or Step 4 as required. At least two TCT’s are required before the next acquisition starts.

NOTE

1. To obtain an accurate value, it is necessary to avoid any data transition on the I/O pins during AD conversion.

> *2. Order of setting the register:*
> *A. Before setting the AD conversion pins (AISR), the corresponding input channel (ADIS2~0) and ADC power supply (ADPD = 1) must be set.*
> *B. After the AD conversion is completed, turn off the AD conversion pin function (AISR).*
> *For actual program settings, refer to the section in red in the demonstration program.*
> ***If the procedure described above is not followed, the AD conversion value may not come out as expected.***
> *3. AD pins that are not data-converted must be set as high-impedance input pins. For example, if P60, P61, and P62 (AD0~2) are AD pins, P61 and P62 must be set as high-impedance input pins to begin P60 AD data conversion. Similarly, to begin P61 AD data conversion, P60 and P62 must be set as high-impedance input pins. [P60, P61, and P62 can be set as high-impedance input pins during program initialization].*

■ Demonstration Programs

```
; Define System Control Register
IAR         ==      0x00          ; Indirect Addressing Register
SR          ==      0x03          ; Status Register
PORT5       ==      0x05
PORT6       ==      0x06
WUPC        ==      0x0A          ; Wake-up Control Register
ISR1        ==      0x0F          ; Interrupt Status Flag Register

; Define I/O Control Register
PORT6       ==      0x06
IOCR6       ==      0x06          ; I/O Control Register of Port 6

; Define ADC Control Register
ADDH        ==      0x08          ; The contents are the results of
                                  ; ADC[11:8]
ADDL        ==      0x09          ; The contents are the results of
                                  ; ADC[7:0]
AISR        ==      0x05          ; ADC Input Channel Select
                                  ; Register
ADCON       ==      0x06          ; ADC Control Register 1
 ADRUN      ==     ADCON.4        ; ADC Run Control
 ADPD       ==     ADCON.3        ; ADC Power Control
ADCON2      ==      0x07          ; ADC Control Register 2
 ADLPFEN    ==     ADCON2.7       ; ADC Low Pass Filter

; Define General Purpose Register
ADCTMP0     ==      0x20
ADCTMP1     ==      0x21

; Program begins
ORG         0x00                  ; Initial address
JMP         INITIAL
ORG         0x30                  ; ADC Interrupt Vector
JMP         ADC_INT
;
;  (User program code)
;
ADC_INT;
BANK    2
MOV         A, ADDH               ; Read A/D Converter High Byte
                                  ; Data Register
```

```
MOV         ADCTMP0, A
MOV         A,    ADDL          ; Read A/D Converter Low Byte Data
                                ; Register
MOV         ADCTMP1, A
BC          ADIF
BC          AISR.2              ; Disable P62(AD2) Analog Input
                                ; Pin function
RETI

INITIAL:
MOV         A, @0xFF            ; Set PORT6 to High Impedance
                                ; Input Pin
MOV         IOCR6, A
MOV         A, @0B00001000      ; Turn on AD Power Supply (ADPD =
                                ; 1) and set clock
                                ; Set clock frequency fosc/4
MOV         ADCON, A
MOV         A, @0x0A            ; Sample and Hold timing is 8 TAD
                                ; ADC Internal reference voltage
                                ; is 3.072V
MOV         ADCON2, A
CALL   DELAY_10US
BS          ADLPFEN
BS          ADWE                ; Enable ADC wake-up function bit
                                ; ADWK
BS          ADIE                ; Enable the ADC interrupt
                                ; function bit ADIE
ENI                             ; Enable interrupt function

EN_ADC:
MOV         A, @0xF8
AND         ADCON, A
MOV         A, @0x02            ; Select AD2 as the ADC input
                                ; channel
OR          ADCON, A
BS          AISR.2              ; Enable P62 (AD2) as analog input
                                ; pin
BS          ADRUN               ; Run ADC
SLEP

; If using interrupt function, the following can be ignored
;
; (User program select)
;
POLLING:
JBS         ADIF
JMP         POLLING
MOV         A, ADDH
MOV         ADCTMP0, A
MOV         A, ADDL
MOV         ADCTMP1, A
BC          ADIF
BC          AISR.2              ; Turn off P54(AD2) Analog Input
                                ; Pin function
```

6.9 Timer/Counter 1 (TM1)

6.9.1 Timer/Counter Mode

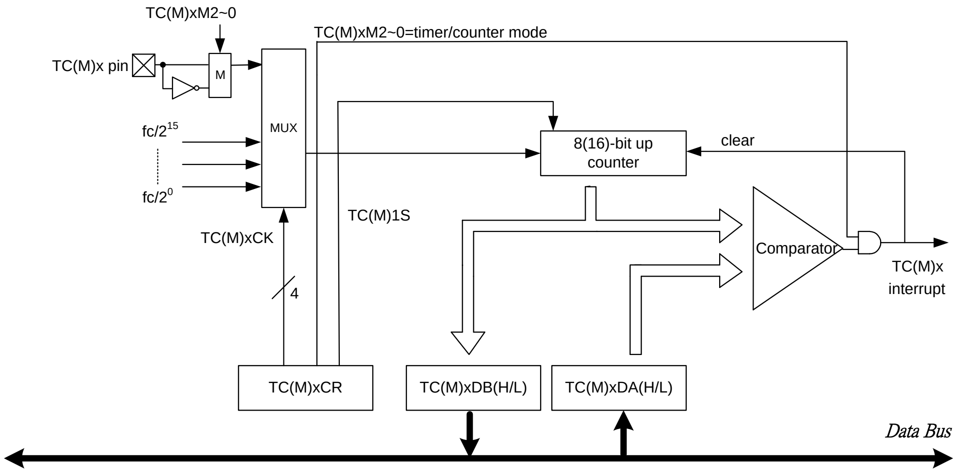


Figure 6-15(a) Timer/Counter Mode Block Diagram

In Timer/Counter mode, counting up is performed using internal clock or TC(M)x pin. When the contents of the up-counter match with the TC(M)xDA, interrupt is generated and the counter is cleared. Counting up resumes after the counter is cleared. The current contents of the up-counter are loaded into TC(M)xDB by setting TC(M)xRC to "1".

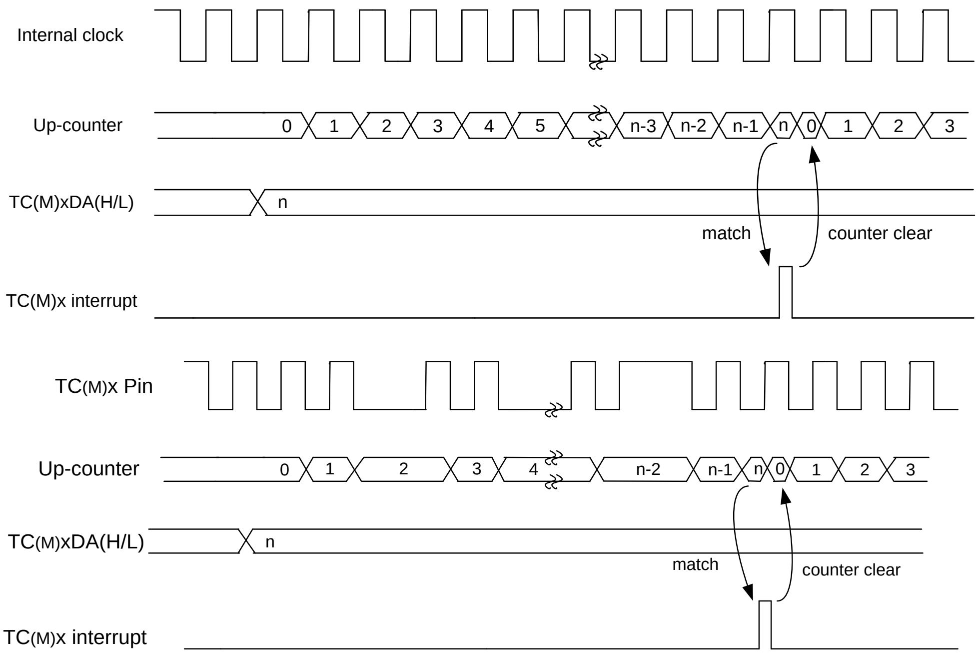


Figure 6-15(b) Timer/Counter Mode Waveform

6.9.2 Window Mode

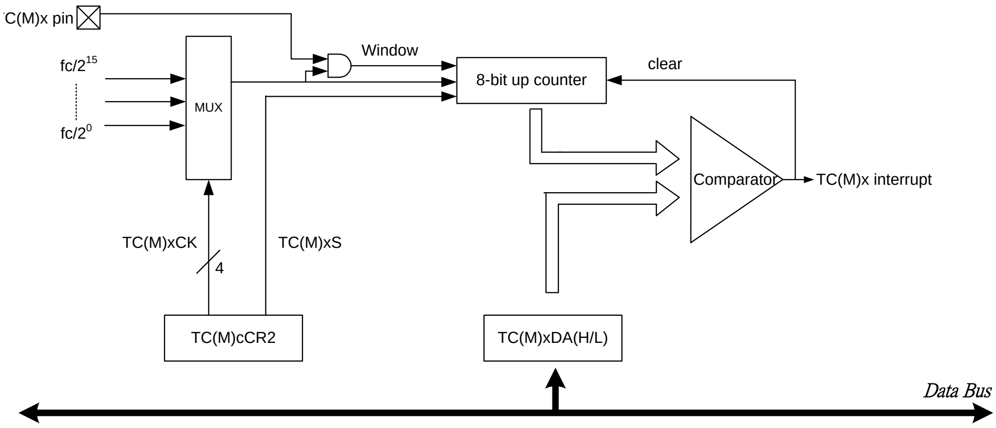


Figure 6-16(a) Window Mode Block Diagram

In Window mode, counting up is performed on a rising edge of the pulse that is logical AND of an internal clock and the TC(M)x pin (window pulse). When the contents of the up-counter match with the TC(M)xDA, interrupt is generated and the counter is cleared. The frequency (window pulse) must be lower than the selected internal clock.

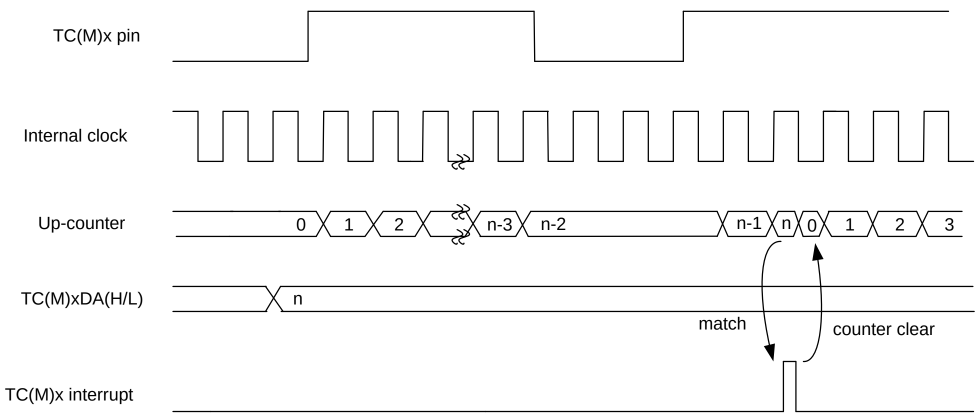


Figure 6-16(b) Window Mode Waveform

6.9.3 Capture Mode

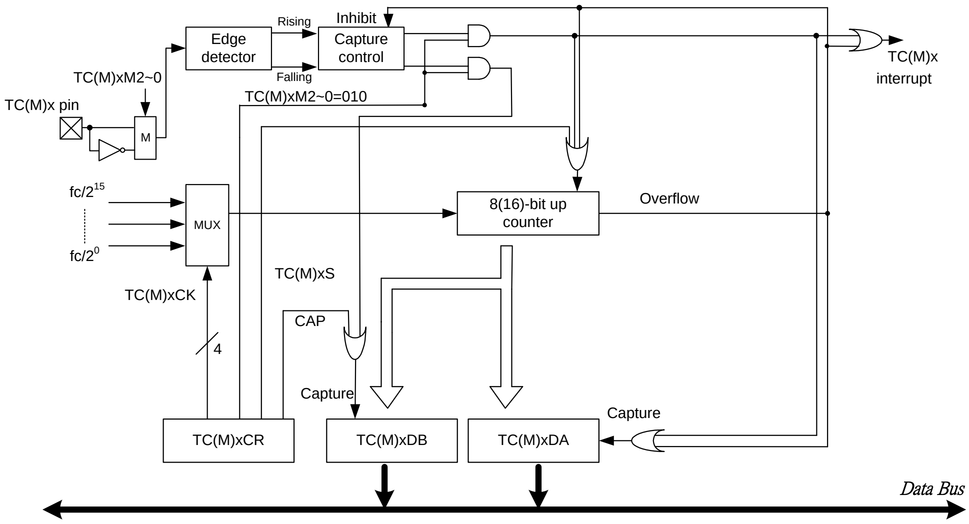


Figure 6-17(a) Capture Mode Block Diagram

In Capture mode, pulse width, period and duty of the TC(M)x input pin are measured, which can be used to decode the remote control signal . The counter is free running by the internal clock. On a rising (falling) edge of the TC(M)x pin, the contents of the counter is loaded into TC(M)xDA, then the counter is cleared and interrupt is generated. On a falling (rising) edge of the TM1 pin, the contents of the counter are loaded into TC(M)xDB. Meanwhile, the counter is still counting. Once the next rising edge of the TC(M)x pin is triggered, the contents of the counter are loaded into TC(M)xDA, the counter is cleared and interrupt is generated once again. If an overflow before the edge is detected, the FFH is loaded into TC(M)xDA and an overflow interrupt is generated. During interrupt processing, overflows can be detected by checking if the TC(M)xDA value is FFH. After an interrupt (capture to TC(M)xDA or overflow detection) is generated, capture and overflow detection are halted until TC(M)xDA is read out.

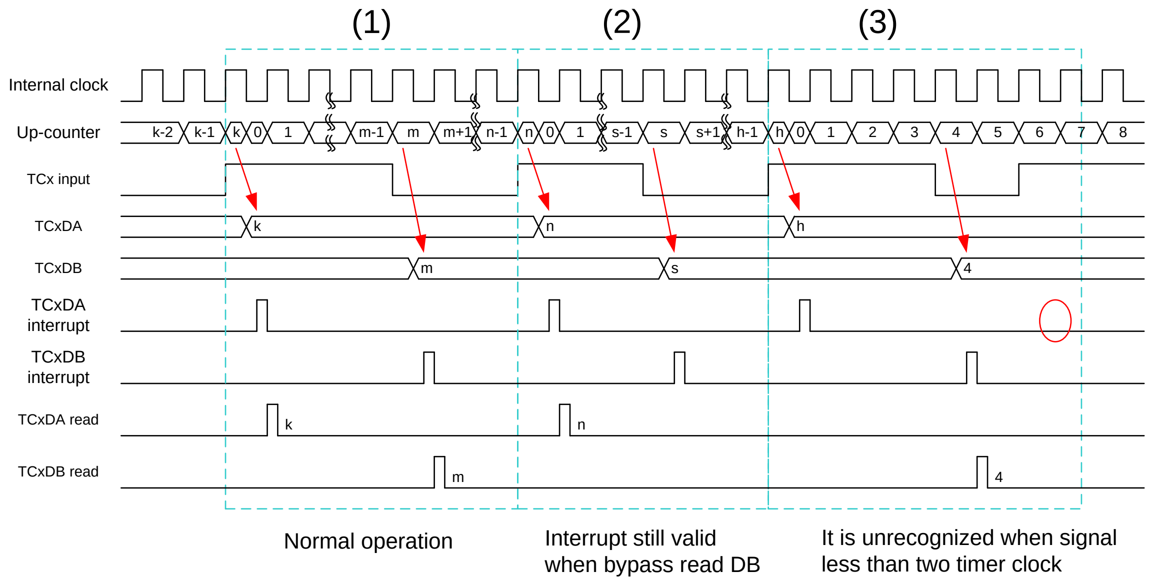


Figure 6-17(b) Capture Mode Waveform

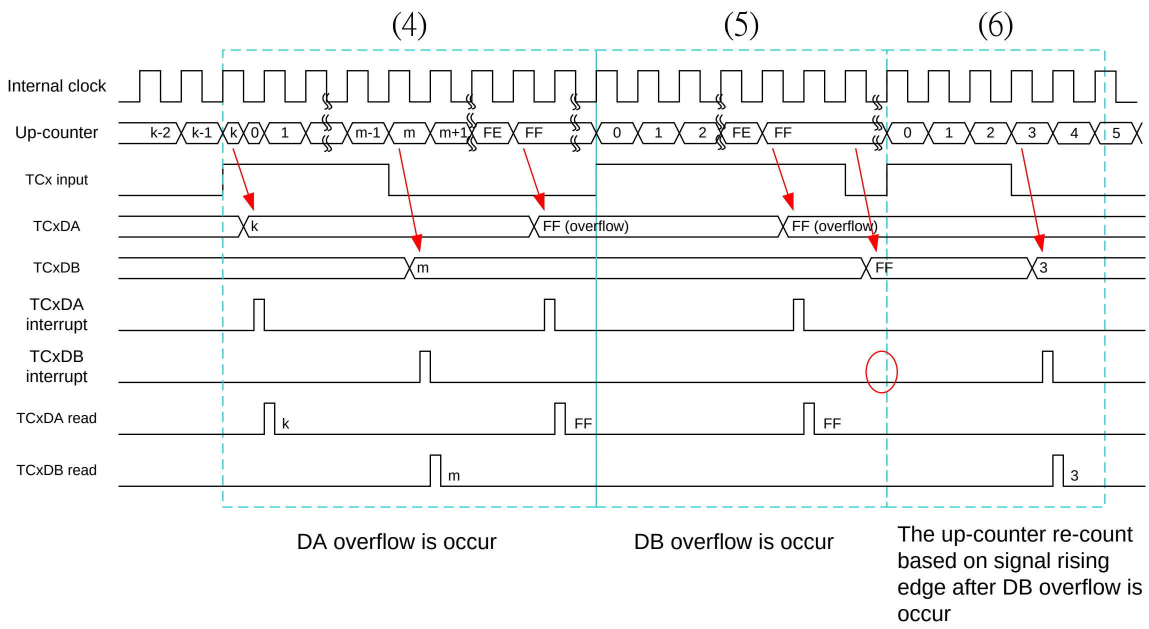
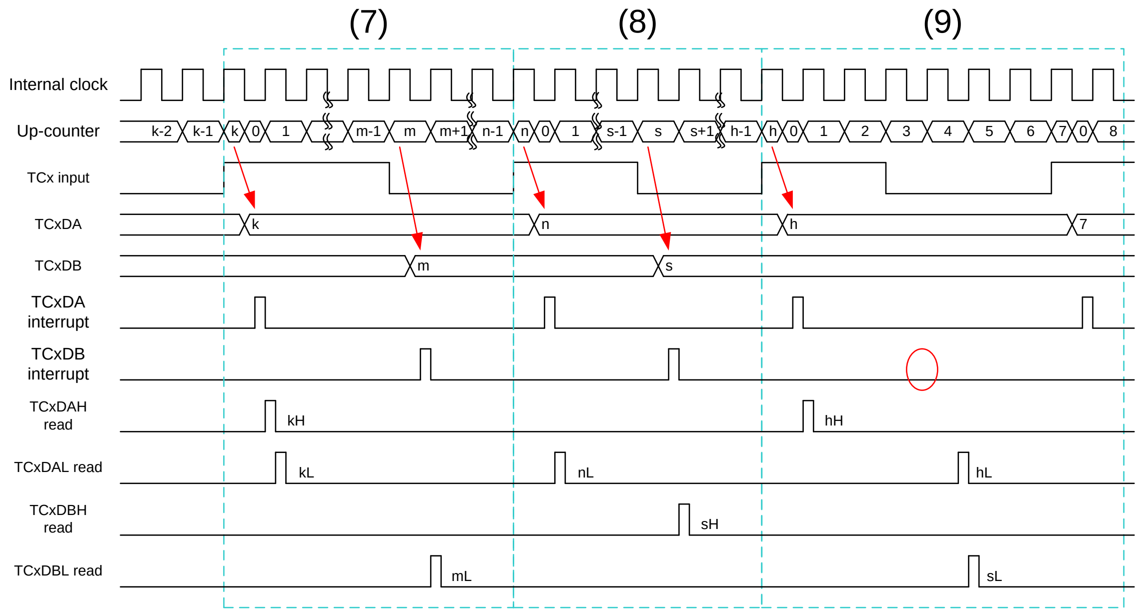


Figure 6-17(c) Capture Mode Waveform



Only read low byte of DB | Only read low byte of DA | Interrupt is invalid when read high byte only

Figure 6-17(d) Capture Mode Waveform

6.9.4 Programmable Divider Output Mode and Pulse Width Modulation Mode

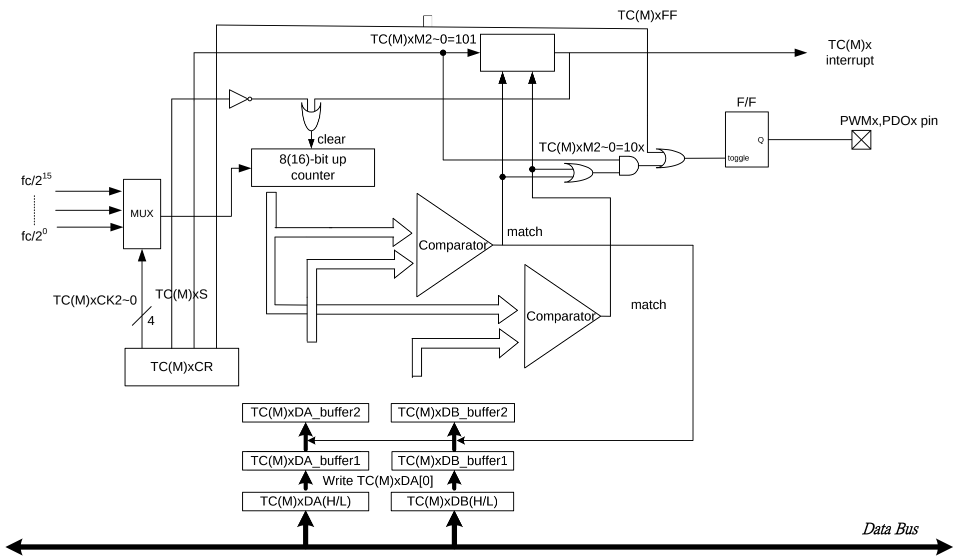


Figure 6-18(a) PDO/PWM Mode Block Diagram

■ **Programmable Divider Output (PDO)**

In Programmable Divider Output (PDO) mode, counting up is performed using internal clock. The contents of the TC(M)xDA are compared with the contents of the up-counter. The F/F output is toggled and the counter is cleared each time a match is found. The F/F output is inverted and output to PDO pin. This mode can generate 50% of duty pulse output. The PDO pin is initialized to "**0**" during reset and a TC(M)x interrupt is generated each time the PDO output is toggled.

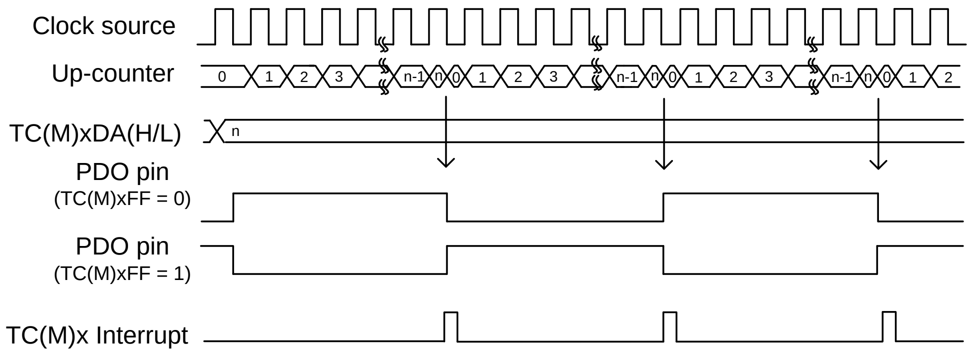


Figure 6-18(b) PDO Mode Waveform

- **Pulse Width Modulation (PWM)**

In Pulse Width Modulation (PWM) Output mode, counting up is performed using the internal clock with prescaler. The Duty of PWMx is controlled by TC(M)xDB, and the period of PWMx is controlled by TC(M)xDA. The pulse at the PWMx pin is held to a high level as long as TC(M)xS=1 or timerx matches TC(M)xDA, while the pulse is held to a low level as long as Timerx matches TC(M)xDB. Once TC(M)xFF is set to 1, the signal of PWMx is inverted. A TC(M)x interrupt is generated and defined by TC(M)xIS. On the other hand, the TC(M)xDA and TC(M)xDB can be written at any time, but the data of TC(M)xDA and TC(M)xDB are latched only at writing TC(M)xDA0. Therefore, the new duty and new period of PWM appear at the PMW pin at the last period–match.

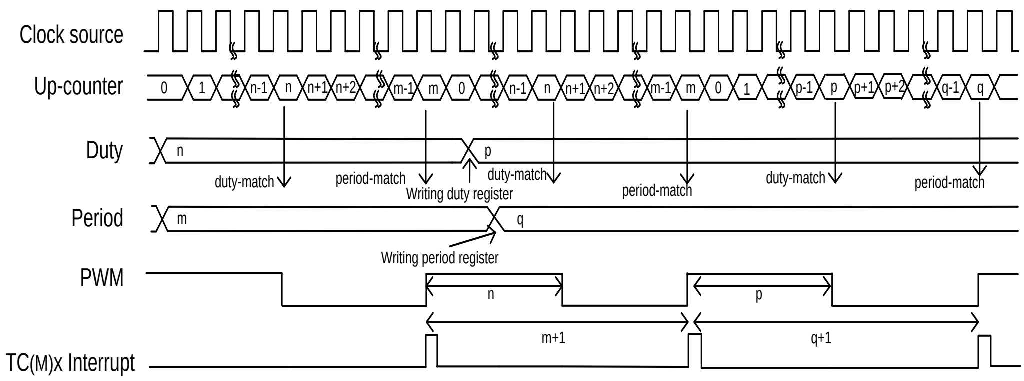


Figure 6-18(c) PWM Mode Waveform

6.9.5 Buzzer Mode

The TC(M)x pin outputs the clock after dividing the frequency.

6.10 Timer/Counter 3 (TC3)

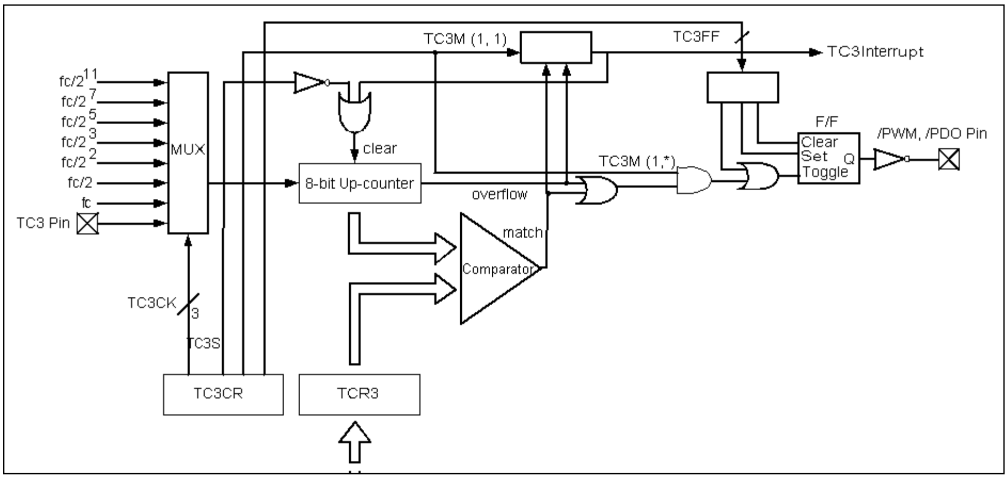


Figure 6-19 Timer/Counter 3 Configuration

In Timer mode, counting up is performed using the internal clock (rising edge trigger). When the contents of the up-counter matched with the contents of TCR3, interrupt is then generated and the counter is cleared. Counting up resumes after the counter is cleared.

In Counter mode, counting up is performed using the external clock input pin (TC3). When the contents of the up-counter matched with the contents of TCR3, interrupt is then generated and the counter is cleared. Counting up resumes after the counter is cleared.

In Programmable Divider Output (PDO) mode, counting up is performed using the internal clock. The contents of TCR3 are compared with the contents of the up-counter. The F/F output is toggled and the counter is cleared each time a match is found. The F/F output is inverted and output to /PDO pin. This mode can generate 50% duty pulse output. **The F/F can be initialized by program and it is initialized to "0" during reset.** A TC3 interrupt is generated each time the /PDO output is toggled.

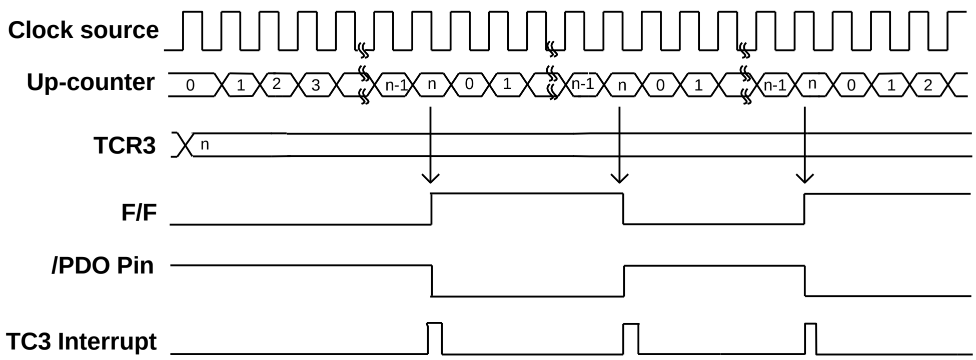


Figure 6-20 PDO Mode Timing Diagram

In Pulse Width Modulation (PWM) Output mode, counting up is performed using the internal clock. The contents of TCR3 are compared with the contents of the up-counter. The F/F is toggled when a match is found. While the counter is counting, the F/F is toggled again when the counter overflows, after which the counter is cleared. The F/F output is inverted and output to the /PWM pin. A TC3 interrupt is generated each time an overflow occurs. **TCR3 is configured as a 2-stage shift register and during output, will not switch until one output cycle is completed even if TCR3 is overwritten.** Hence, the output can be changed continuously. Also, after data is loaded to TCR3, the TCR3 is shifted for the first time by setting TC3S to "**1**".

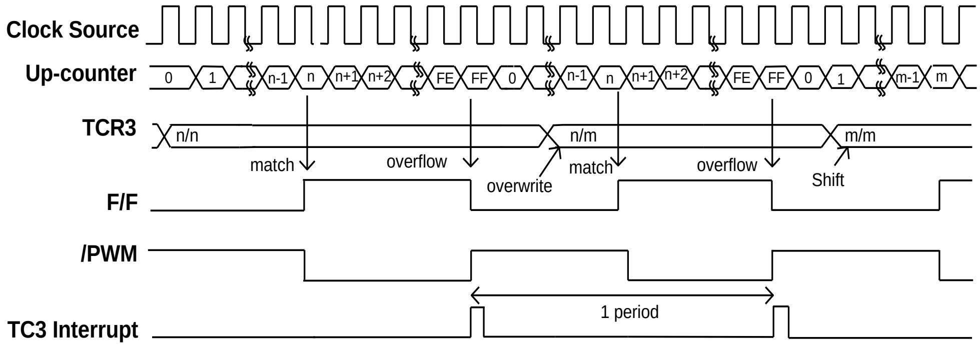


Figure 6-21 PWM Mode Timing Diagram

6.11 UART

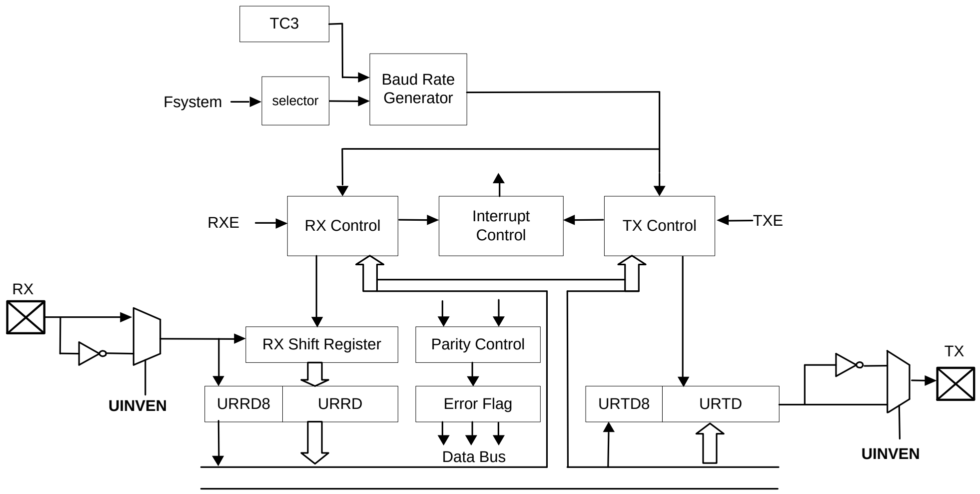


Figure 6-22 UART Functional Block Diagram

In Universal Asynchronous Receiver Transmitter (UART), each transmitted or received character is individually synchronized by framing it with a start bit and stop bit.

Full duplex data transfer is possible since the UART has independent transmit and receive sections. Double buffering for both sections allows the UART to be programmed for continuous data transfer.

The figure below shows the general format of one character sent or received. The communication channel is normally held in the marked state (high). Character transmission or reception starts with a transition to the space state (low).

The first bit transmitted or received is the start bit (low). It is followed by the data bits, in which the least significant bit (LSB) comes first. The data bits are followed by the parity bit. If present, then the stop bit or bits (high) confirm the end of the frame.

In receiving, the UART synchronizes on a falling edge of the start bit. When two or three "0" are detected during three samples, it is recognized as normal start bit and the receiving operation is started.

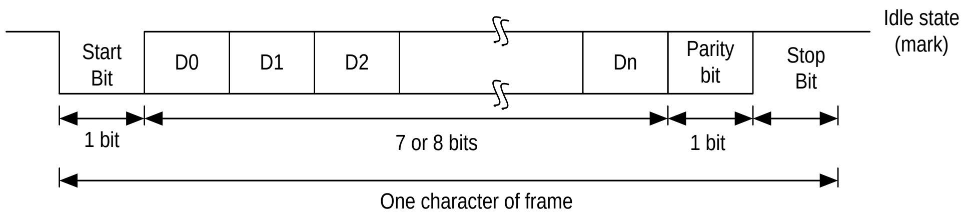


Figure 6-23 Data Format in UART

6.11.1 UART Mode

There are three UART modes. Mode 1 (7 bits data) and Mode 2 (8 bits data) allow the addition of a parity bit. The parity bit addition is not available in Mode 3. Figure 6-24a below shows the data format in each mode.

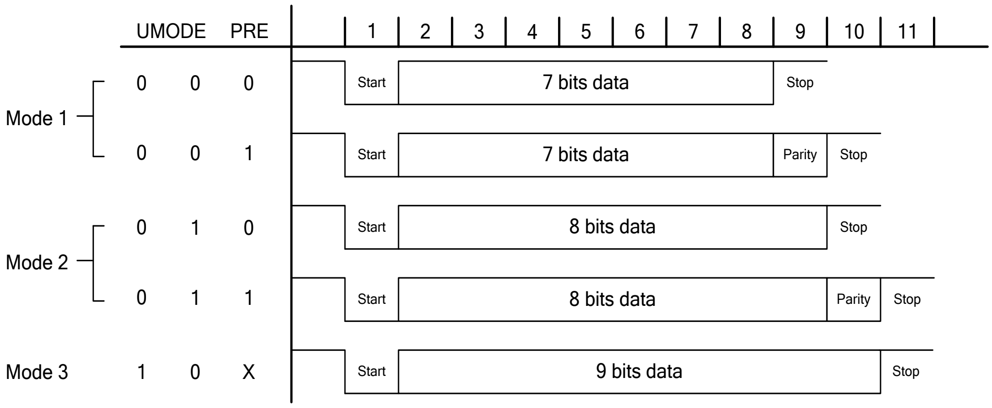


Figure 6-24a UART Model

6.11.2 Transmitting

In transmitting serial data, the UART operates as follows:

1. Set the TXE bit of the URCR register to enable the UART transmission function.
2. Write data into the URTD register and the UTBF bit of the URCR register will be cleared by hardware.
3. Then start transmitting.
4. Serially transmitted data are transmitted in the following order from the TX pin.
5. Start bit: one "**0**" bit is output.
6. Transmit data: 7, 8 or 9 bits data are output from the LSB to the MSB.
7. Parity bit: one parity bit (odd or even selectable) is output.
8. Stop bit: one "**1**" bit (stop bit) is output.

Mark state: output "1" continues until the start bit of the next transmitted data.

After transmitting the stop bit, the UART generates a UTIF interrupt (if enabled).

6.11.3 Receiving

In receiving, the UART operates as follows:

1. Set the RXE bit of the URS register to enable the UART receiving function. The UART monitors the RX pin and synchronizes internally when it detects a start bit.
2. Receive data is shifted into the URRD register in the order from LSB to MSB.
3. The parity bit and the stop bit are received. After one character is received, the URBF bit of the URS register will be set to "**1**". This means UART interrupt will occur.
4. The UART makes the following checks:
   (a) Parity check: The number of "1" of the received data must match the even or odd parity setting of the EVEN bit in the URS register.
   (b) Frame check: The start bit must be "0" and the stop bit must be "1".
   (c) Overrun check: The URBF bit of the URS register must be cleared (that means the URRD register should be read out) before the next received data is loaded into the URRD register.

   If any checks failed, the UERRIF interrupt will be generated (if enabled), and an error flag is indicated in PRERR, OVERR or FMERR bit. The error flag should be cleared by software, otherwise, UERRIF interrupt will occur when the next byte is received.
5. Read received data from URRD register. And URBF bit will be set by hardware.

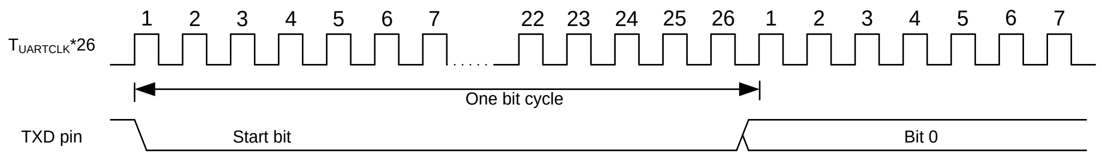
6.11.4 Baud Rate Generator

The baud rate generator is comprised of a circuit that generates a clock pulse to determine the transfer speed for transmission/reception in the UART.

The BRATE2~BRATE0 bits of the URC register can determine the desired baud rate.

6.11 .5 UART Timing

1. Transmission Counter Timing:



2. Receiving Counter Timing:

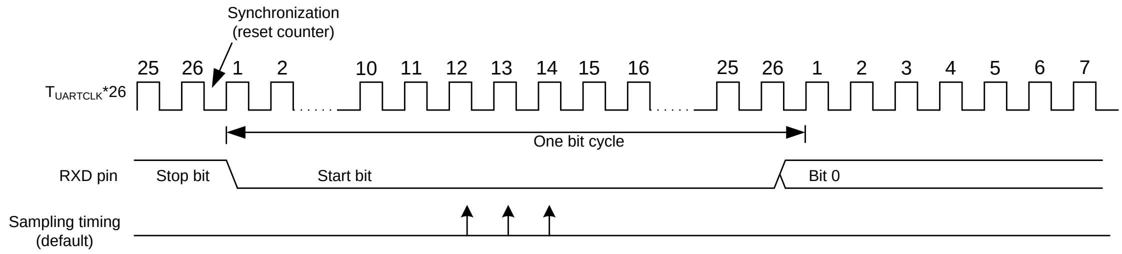


Figure 6-24b UART Timing Diagrams

6.12 Comparator

The comparator can be utilized to wake up EM78F811N from Sleep mode. Figure 6-25 shows the comparator block diagram.

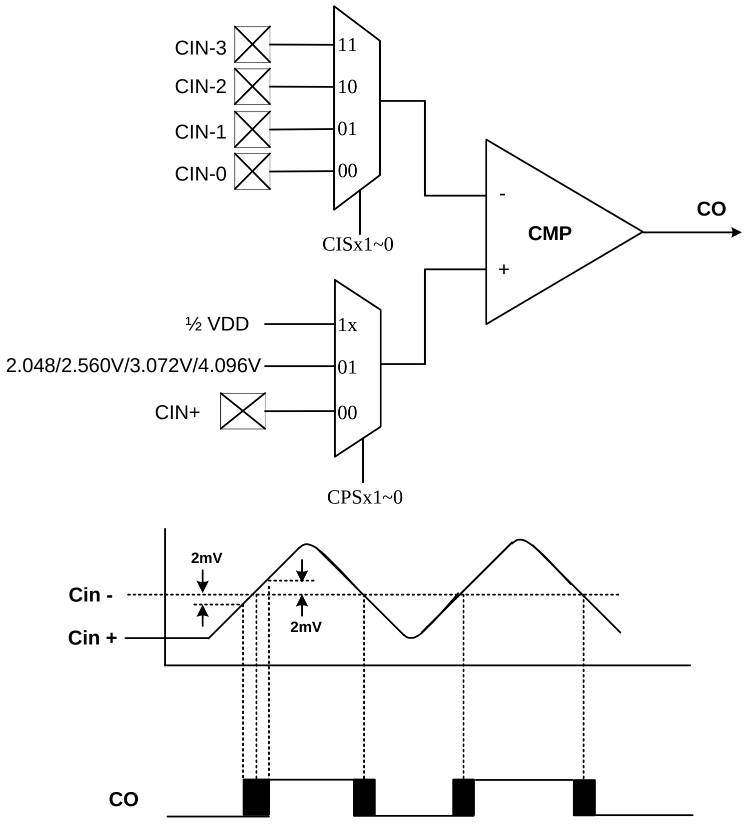


Figure 6-25 Comparator Block Diagram

6.12.1 External Reference Signal

The analog signal that is presented at Cin- is compared to the signal at Cin+, and the digital output (CO) of the comparator is adjusted in accordance with the following considerations:

- The reference signal must be between Vss and Vdd.
- The reference voltage can be applied to either pin of the comparator.
- Threshold detector applications may be of the same reference.
- The comparator can operate from the same or different reference source.

6.12.2 Internal Reference Source

The Cin+ support four internal reference voltages (2.048V、2.560V、3.072V and 4.096V) and 1/2 VDD. When the internal reference is selected, the Input offset voltage at about 15mV. Note that the comparator is not permitted to use internal reference when AD is working and is selected as source for Vref.

6.12.3 Comparator Outputs

- The compared result is stored in the CPOUT2 of R7 Bit 4 of Bank 3.
- The comparator is output to CO2 (P80) by programming Bit 3, Bit 2 <COS21, COS20> of Register R7 Bank 3.

The Figure below shows the comparator output block diagram.

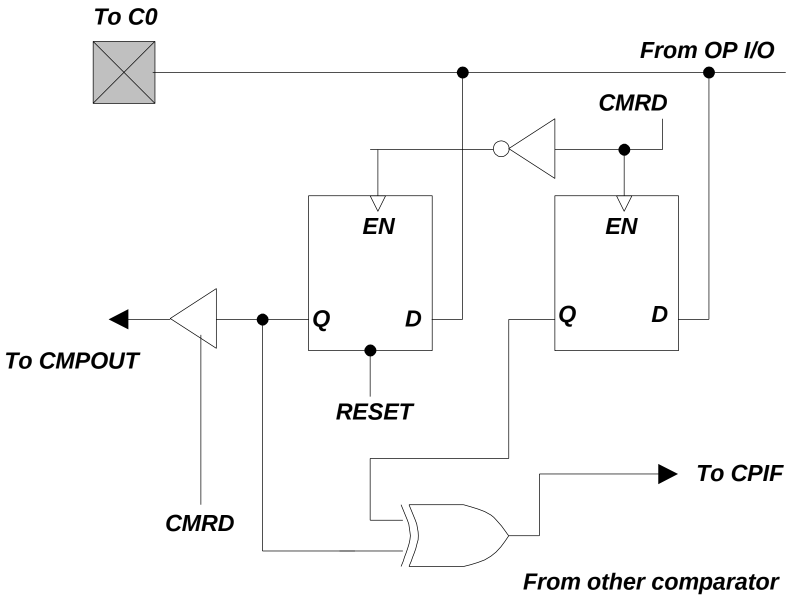


Figure 6-26 Comparator Output Configuration

6.12.4 Interrupt

- CMP2IE (IOCE.7) must be enabled for the “ENI” instruction to take effect.
- Interrupt triggers whenever a change occurs on the comparator output pin.
- The actual change on the pin can be determined by reading Bit CPOUT2 (R7.4, Bank 3).
- CMP2IF (RF.7, Bank 1), the comparator interrupt flag, can only be cleared by software.

6.12.5 Wake-up from Sleep Mode

- If enabled, the comparator remains active and the interrupt remains functional, even in Sleep mode.
- If a mismatch occurs, the interrupt will wake up the device from Sleep mode.
- The power consumption should be taken into consideration for the benefit of energy conservation.
- If the function is unemployed during Sleep mode, turn off the comparator before entering into sleep mode.

6.12.6 Comparator Initialization Steps

- Select CMP inverting end channel (CIS21~CIS20).
- Select CMP Non-inverting end channel (CPS22~CPS20).
- Wait at least 10us when CPS22~CPS20 is 01.
- Set the ADLPFEN when CPS22~CPS20 is 01.
- Enable CMP, set COS21~COS20 to 01 or 1x.

6.13 Oscillator

6.13.1 Oscillator Modes

The EM78F811N device can be operated in four different oscillator modes, including Internal RC oscillator mode (IRC), External RC oscillator mode (ERC), High Crystal oscillator mode (HXT), and Low Crystal oscillator mode (LXT). User can select one of such modes by programming OSC2, OSC1, and OSC0 in the Code Option register. Table below depicts how these modes are defined.

■ **Oscillator Modes defined by OSC2 ~ OSC0**

Mode	OSC2	OSC1	OSC0
IRC (Internal RC oscillator mode); P55, P54 acts as I/O pin	**0**	**0**	**0**
HXT (High Crystal oscillator mode)	**0**	**0**	**1**
LXT1 (Low Crystal 1 oscillator mode)	**0**	**1**	**0**
LXT2 (Low Crystal 2 oscillator mode)	**0**	**1**	**1**
XT (Crystal oscillator mode)	**1**	**0**	**0**
IRC (Internal RC oscillator mode); P55 acts as I/O pin P54 acts as RCOUT pin	**1**	**0**	**1**
ERC (External RC oscillator mode); P55 acts as ERCin pin P54 acts as I/O pin	**1**	**1**	**0**
ERC (External RC oscillator mode); P55 acts as ERCin pin P54 acts as RCOUT pin with Open-drain	**1**	**1**	**1**

Note:

1) Frequency range of HXT mode is dependent on the HXTS bit

2) Frequency range of XT mode is 6 MHz ~ 1 MHz

3) Frequency range of LXT1 mode is 1 MHz ~ 100 kHz.

4) Frequency range of LXT2 mode is 32.768 kHz.

OSCI and OSCO are used in LXT2, LXT1, XT, HXT, and ERC modes. They cannot be used as normal I/O pins.

In IRC mode, P55 is used as normal I/O pin.

The up-limited operation frequency of the crystal/resonator on the different VDD is listed in the following table.

■ **Summary of Maximum Operating Speeds**

Conditions	VDD	Max. Fxt. (MHz)
Two cycles with two clocks	2.2	4.0
	2.5	8.0
	4.0	16.0

6.13.2 Crystal Oscillator/Ceramic Resonators (Crystal)

The EM78F811N can be driven by an external clock signal through the OSCI pin as illustrated below.

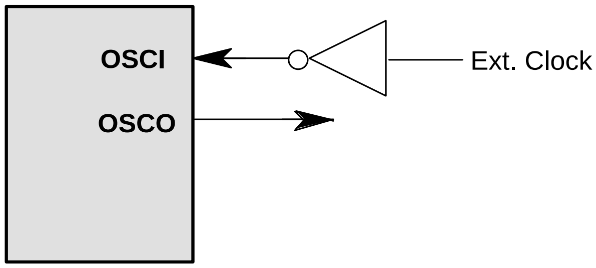


Figure 6-27 Circuit for External Clock Input

In most applications, Pin OSCI and Pin OSCO can be connected with a crystal or ceramic resonator to generate oscillation as depicted in the figure below. The same thing applies whether it is in the HXT mode or in the LXT mode.

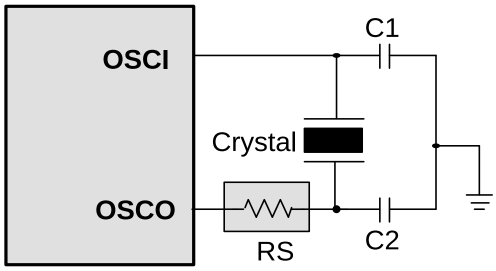


Figure 6-28 Circuit for Crystal/Resonator

The following table provides the recommended values of C1 and C2. Since each resonator has its own attribute, you should refer to its specification for appropriate values of C1 and C2. A serial resistor RS, may be necessary for AT strip cut crystal or in low frequency mode.

■ **Capacitor Selection Guide for Crystal Oscillator or Ceramic Resonator**

Oscillator Type	Frequency Mode	Frequency	C1 (pF)	C2 (pF)
Ceramic Resonators	LXT1 (100K~1 MHz)	100 kHz	45pF	45pF
		200 kHz	20pF	20pF
		455 kHz	20pF	20pF
		1.0 MHz	20pF	20pF
	XT (1M~6 MHz)	1.0 MHz	25pF	25pF
		2.0 MHz	20pF	20pF
		4.0 MHz	20pF	20pF
Crystal Oscillator	LXT2 (32.768kHz)	32.768 kHz	40pF	40pF
	LXT1 (100K~1 MHz)	100 kHz	45pF	45pF
		200 kHz	20pF	20pF
		455 kHz	20pF	20pF
		1.0 MHz	20pF	20pF
	XT (1~6 MHz)	455 kHz	30pF	30pF
		1.0 MHz	20pF	20pF
		2.0 MHz	20pF	20pF
		4.0 MHz	20pF	20pF
		6.0 MHz	20pF	20pF
	HXT (HXTS=0) (6~16 MHz)	6.0 MHz	25pF	25pF
		8.0 MHz	20pF	20pF
		10.0 MHz	20pF	20pF
		12.0 MHz	20pF	20pF
		16.0 MHz	15pF	15pF
	HXT (HXTS=1) (12~16 MHz)	12.0 MHz	20pF	20pF
		16.0 MHz	15pF	15pF

6.13.3 External RC Oscillator Mode

For some applications that do not require a very precise timing calculation, the RC oscillator (Figure 6-26 below) offers a cost-effective oscillator configuration. Nevertheless, it should be noted that the frequency of the RC oscillator can be affected by the supply voltage, the values of the resistor (Rext), the capacitor (Cext), and even by the operation temperature. Moreover, the frequency also changes slightly from one chip to another due to manufacturing process variation.

In order to maintain a stable system frequency, the values of the Cext should not be less than 20pF, and that of Rext should not be greater than 1MΩ. If they cannot be kept under these ranges, the frequency can be easily affected by noise, humidity, and leakage.

The smaller the Rext in the RC oscillator, the faster its frequency will be. However, when a very low Rext value is used, for instance, 1KΩ; the oscillator will become unstable since the NMOS cannot correctly discharge the capacitance current.

Based on the above conditions, it must be kept in mind that all of the supply voltage, the operation temperature, the components of the RC oscillator, the package types, and the PCB layout, could affect the system frequency.

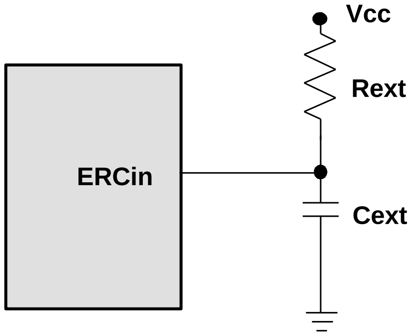


Figure 6-29 External RC Oscillator Mode Circuit

■ **RC Oscillator Frequencies**

Cext	Rext	Average Fosc 5V, 25°C	Average Fosc 3V, 25°C
20 pF	3.3k	1.75 MHz	1.6 MHz
	5.1k	1.25 MHz	1.15 MHz
	10k	0.65 MHz	0.625 MHz
	100k	70 kHz	70 kHz
100 pF	3.3k	0.635 MHz	0.605 MHz
	5.1k	425 kHz	410 kHz
	10k	225 kHz	225 kHz
	100k	24 kHz	25 kHz
300 pF	3.3k	280 kHz	270 kHz
	5.1k	185 kHz	180 kHz
	10k	98 kHz	96 kHz
	100k	10 kHz	10 kHz

Note:

Measured based on DIP packages. These are theoretical values intended for design reference only.

6.13.4 Internal RC Oscillator Mode

The EM78F811N offers a versatile internal RC mode with default frequency value of 4MHz. Internal RC oscillator mode has other frequencies (16 MHz、8 MHz、1MHz and 455KHz) that can be set by Code Option Word1<4,3,2> or switch by Bank1 R8<7,6,5>, RCM1 and RCM0. All these main frequencies can be calibrated by programming the Code Option.

IRC Power	Internal RC Frequency	Temperature (-40°C~85°C)	Voltage (2.2V~5.5V)	Process	Total
Int. Regulator	4 MHz	± 3.75%		± 1%	± 4.75%
	16 MHz	± 3.75%		± 1%	± 4.75%
	8 MHz	± 3.75%		± 1%	± 4.75%
	1 MHz	± 3.0%		± 1%	± 4%
	455KHz	± 3.0%		± 1%	± 4%

**The drift rate is based on NUWriter trim only, detail refer to DC Electrical Characteristics

6.14 Code Option Register

The EM78F811N has a Code Option Word that is not part of the normal program memory. The option bits cannot be accessed during normal program execution.

Code Option Register and Customer ID Register arrangement distribution**:**

Word 0	Word 1	Word 2
Bit 12~Bit 0	Bit 12~Bit 0	Bit 12~Bit 0

6.14.1 Code Option Register (Word 0)

Word 0													
Bit Num	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Name	**HXTS**	**NRHL**	**NRE**	**RESETENB**	**CLKS1**	**CLKS0**	**ENWDTB**	**OSC2**	**OSC1**	**OSC0**	**EEPR**		
Default	0	0	0	0	0	0	0	0	0	0	1		

Bit 12 (HXTS): Select frequency range for HXT mode.

0: HXT2: Frequency range of HXT mode is 12 MHz ~ 6 MHz

1: HXT1: Frequency range of HXT mode is 16 MHz ~ 12 MHz

Bit 11 (NRHL): Noise rejection high/low pulse define bit. INT pin is a falling edge trigger.

0: Pulses equal to 32/fc [s] are regarded as signal.

1: Pulses equal to 8/fc [s] are regarded as signal.

Bit 10 (NRE): Noise rejection enabled. The INT pin is falling edge triggered.

0: Enable noise rejection.

1: Disable noise rejection.

> **NOTE:**
> *The noise rejection function is always disabled in Low Crystal Oscillator (LXT2) and Sleep mode.*

Bit 9 (RESETENB): Reset pin enable bit

0: P83 set to I/O pin

1: P83 set to /RESET pin

Bit 8 ~ Bit 7 (CLKS1 ~ CLKS0): Instruction period option bit

Instruction Period	CLKS1	CLKS0
4 clocks	**0**	**0**
2 clocks	**0**	**1**
8 clocks	**1**	**0**
16 clocks	**1**	**1**

Refer to Section 6.16, *Instruction Set*.

Bit 6 (ENWDTB): Watchdog timer enable bit

0: Disable

1: Enable

Bit 5 ~ Bit 3 (OSC2 ~ OSC0): Oscillator Mode Selection bits

Mode	OSC2	OSC1	OSC0
IRC (Internal RC oscillator mode); P55, P54 acts as I/O pin	**0**	**0**	**0**
HXT (High Crystal oscillator mode)	**0**	**0**	**1**
LXT1 (Low Crystal 1 oscillator mode)	**0**	**1**	**0**
LXT2 (Low Crystal 2 oscillator mode)	**0**	**1**	**1**
XT (Crystal oscillator mode)	**1**	**0**	**0**
IRC (Internal RC oscillator mode); P55 acts as I/O pin P54 acts as RCOUT pin	**1**	**0**	**1**
ERC (External RC oscillator mode); P55 acts as ERCin pin P54 acts as I/O pin	**1**	**1**	**0**
ERC (External RC oscillator mode); P55 acts as ERCin pin P54 acts as RCOUT pin with Open-Drain	**1**	**1**	**1**

Note: *1. Frequency range of HXT mode is dependent on the HXTS bit*
2. Frequency range of XT mode is 6 MHz ~ 1 MHz
3. Frequency range of LXT1 mode is 1 MHz ~ 100kHz
4. Frequency range of LXT2 mode is 32.768kHz

Bit 2 ~ Bit 0 (Protect): EEPROM Protect bit. Protect type is as follows**:**

EEPR	EEPROM Protect
1	Enable
0	Disable

6.14.2 Code Option Register (Word 1)

Word 1													
Bit Num	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	COBS 0	–	–	HLP	–	–	–	–	RCM2	RCM1	RCM0	LVR1	LVR0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit 12 (COBS0): IRC mode select bit

0: IRC frequency select from code option

1: IRC frequency select from register.

Bit 11: Not used, set to "**1**" all the time

Bit 10: Not used, set to "**0**" all the time

Bit 9 (HLP): Power consumption selection

0: Normal power consumption, applies to working frequency above 1MHz.

1: Low power consumption, applies to working frequency at 1MHz or below 1MHz.

Bit 8 ~ Bit 5: Not used, set to "**0**" all the time

Bit 4 ~ Bit 2 (RCM2 ~ RCM0): RC mode select bits

RCM 2	RCM 1	RCM 0	Frequency (Hz)
0	0	0	4M
0	0	1	16M
0	1	0	8M
0	1	1	455K
1	X	x	1M

Bit 1 ~ Bit 0 (LVR1 ~ LVR0): Low Voltage Reset Enable bits

LVR1	LVR0	Reset Level	Release Level
0	**0**	NA	NA
0	**1**	2.5V	2.7V
1	**0**	3.5V	3.7V
1	**1**	4.0V	4.2V

Note:
LVR1, LVR0="0, 0" : LVR disable, power-on reset point of EM78F811N is 1.9~2.0V.
LVR1, LVR0="0, 1" : If Vdd <2.5V, the EM78F811N will reset.
LVR1, LVR0="1, 0" : If Vdd <3.5V, the EM78F811N will reset.
LVR1, LVR0="1, 1" : If Vdd <4.0V, the EM78F811N will reset.

6.14.3 Customer ID Register (Word 2)

Word 2													
Bit Num	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Name	**SFS**	**–**	**–**	**–**	**–**	**–**	**Shcksel1**	**Shcksel0**	**ID4**	**ID3**	**ID2**	**ID1**	**ID0**
Default	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit 12 (SFS): Sub frequency select bit

0: 16KHz.

1: 128KHz.

Bit 11: Not used, set to "**0**" all the time.

Bit 9 ~ 8: Not used, set to "**0**" all the time.

Bit 7: Not used, set to "**1**" all the time.

Bit 6 ~ 5 (Shcksel1 ~ 0): System hold clock select bits.

Shcksel1	Shcksel0	System hold clock
0	0	8 clock
0	1	4 clock
1	0	16 clock
1	1	32 clock

Bit 4 ~ 0 (ID4 ~ 0): Customer's ID code.

6.15 Power-on Considerations

No microcontroller is guaranteed to start operating properly before the power supply stabilizes. The EM78F811N has an on-chip Power-on Voltage Detector (POVD) with a detecting level of 1.9V~2.0V. It will work well if Vdd is rising quick enough (50ms or less). In many critical applications, however, extra devices are still required to assist in solving power-up problems.

6.16 External Power-on Reset Circuit

The circuit shown below uses an external RC to produce a reset pulse. The pulse width (time constant) should be kept long enough for Vdd to reach minimum operation voltage. This circuit is used when the power supply has a slow rise time. Since the current leakage from the /RESET pin is ± 5 μA, it is recommended that R should not be greater than 40 KΩ in for the /RESET pin voltage to remain at below 0.2V. The diode (D) functions as a short circuit at the moment of power down. The capacitor C will discharge rapidly and fully. The current-limited resistor (Rin) will prevent high current or ESD (electrostatic discharge) from flowing to /RESET pin.

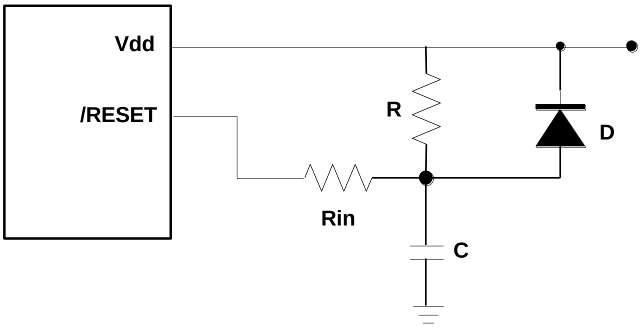


Figure 6-30 External Power-up Reset Circuit

6.17 Residue-Voltage Protection

When the battery is replaced, the device power (Vdd) is taken off but residue-voltage remains. The residue-voltage may trip below Vdd minimum, but not to zero. This condition may cause a poor power-on reset. Figure 6-31 and Figure 6-32 show how to create a proper residue-voltage protection circuit.

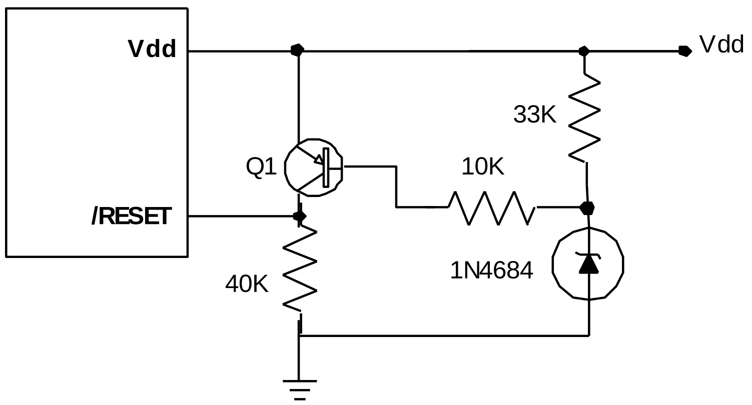


Figure 6-31 Circuit 1 for the Residue Voltage Protection

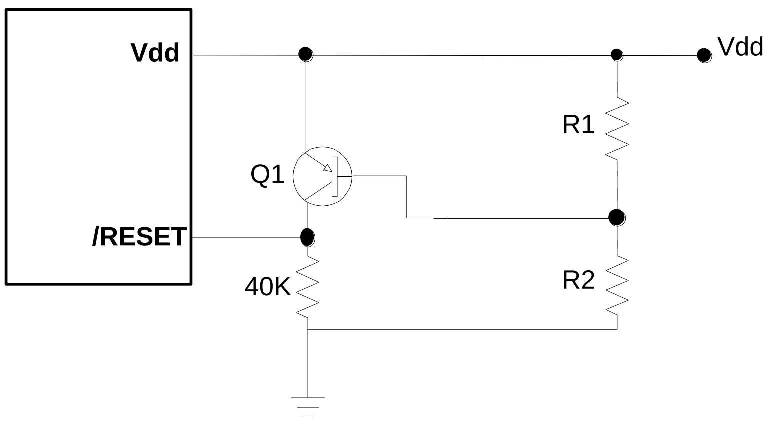


Figure 6-32 Circuit 2 for the Residue Voltage Protection

6.18 Instruction Set

Each instruction in the Instruction Set is a 13-bit word divided into an OP code and one or more operands. Normally, all instructions are executed within one single instruction cycle (one instruction consists of two oscillator periods), unless the program counter is changed by instructions "MOV R2, A", "ADD R2, A", or by instructions of arithmetic or logic operation on R2 (e.g., "SUB R2, A", "BS(C) R2,6", "CLR R2", etc.). In this case, the execution takes two instruction cycles.

If for some reasons, the specification of the instruction cycle is not suitable for certain applications, try to modify the instruction as follows**:**

A) Change one instruction cycle to consist of four oscillator periods.

B) "TBRD", "RET", "RETL", "RETI", or the conditional skip ("JBS", "JBC", "JZ", "JZA", "DJZ", "DJZA") commands which were tested to be true, are executed within two instruction cycles. The instructions that are written to the program counter also take two instruction cycles.

Case A is selected by the Code Option bit called CLKS. One instruction cycle consists of two oscillator clocks if CLKS1&0 is "**01**", and four oscillator clocks if CLKS1&0 is "**00**" (see Section 6.13.1 *(Code Option Register (Word 0)*).

Note that once the four oscillator periods within one instruction cycle is selected as in Case A, the internal clock source for TCC should be CLK = Fc as indicated in Figure 6-7 *(TCC and WDT Block Diagram)* in Section 6.3.

In addition, the Instruction Set has the following features**:**

1) Every bit of any register can be set, cleared, or tested directly.

2) The I/O register can be regarded as general register. That is, the same instruction can operate on the I/O register.

■ Instruction Set Table

The following symbols are used in the following table**:**

R = *Register designator that specifies which one of the registers (including operation and general purpose registers) is to be utilized by the instruction.*

b = *Bit field designator that selects the value for the bit located in the Register R and which affects the operation.*

k = *8 or 10-bit constant or literal value*

Mnemonic	Operation	Status Affected
NOP	No Operation	None
DAA	Decimal Adjust A	C
CONTW	A → CONT	None
SLEP	0 → WDT, Stop oscillator	T, P
WDTC	0 → WDT	T, P
IOW R	A → IOCR	None[1]
ENI	Enable Interrupt	None
DISI	Disable Interrupt	None
RET	[Top of Stack] → PC	None
RETI	[Top of Stack] → PC, Enable Interrupt	None
CONTR	CONT → A	None
IOR R	IOCR → A	None[1]
MOV R,A	A → R	None
CLRA	0 → A	Z
CLR R	0 → R	Z
SUB A,R	R-A → A	Z, C, DC
SUB R,A	R-A → R	Z, C, DC
DECA R	R-1 → A	Z
DEC R	R-1 → R	Z
OR A,R	A ∨ R → A	Z
OR R,A	A ∨ R → R	Z
AND A,R	A & R → A	Z
AND R,A	A & R → R	Z
XOR A,R	A ⊕ R → A	Z
XOR R,A	A ⊕ R → R	Z
ADD A,R	A + R → A	Z, C, DC
ADD R,A	A + R → R	Z, C, DC
MOV A,R	R → A	Z
MOV R,R	R → R	Z
COMA R	/R → A	Z
COM R	/R → R	Z

[1] *This instruction is applicable to IOC5~IOC7, IOCA ~ IOCF only.*

(Continuation)

Mnemonic	Operation	Status Affected
INCA R	R+1 → A	Z
INC R	R+1 → R	Z
DJZA R	R-1 → A, skip if zero	None
DJZ R	R-1 → R, skip if zero	None
RRCA R	R(n) → A(n-1), R(0) → C, C → A(7)	C
RRC R	R(n) → R(n-1), R(0) → C, C → R(7)	C
RLCA R	R(n) → A(n+1), R(7) → C, C → A(0)	C
RLC R	R(n) → R(n+1), R(7) → C, C → R(0)	C
SWAPA R	R(0-3) → A(4-7), R(4-7) → A(0-3)	None
SWAP R	R(0-3) ↔ R(4-7)	None
JZA R	R+1 → A, skip if zero	None
JZ R	R+1 → R, skip if zero	None
BC R,b	0 → R(b)	None[2]
BS R,b	1 → R(b)	None [3]
JBC R,b	if R(b)=0, skip	None
JBS R,b	if R(b)=1, skip	None
CALL k	PC+1 → [SP], (Page, k) → PC	None
JMP k	(Page, k) → PC	None
MOV A,k	k → A	None
OR A,k	A ∨ k → A	Z
AND A,k	A & k → A	Z
XOR A,k	A ⊕ k → A	Z
RETL k	k → A, [Top of Stack] → PC	None
SUB A,k	k-A → A	Z, C, DC
ADD A,k	k+A → A	Z, C, DC
BANK k	K → R4(7:6)	None
TBRD R	If Bank 3 R6.7=0, machine code (7:0) → R Else Bank 3 R6.7=1, machine code (12:8) → R(4:0), R(7:5)=(0,0,0)	None

[2] *This instruction is not recommended for interrupt status register operation.*
If you want to clear Bit0 for interrupt status register (ex: 0xF), use the method below:

```
MOV     A,@0B11111110
AND     0xF,A
```

[3] *This instruction cannot operate under interrupt status register.*

7 On-Chip Debug Support (OCDS)

The MCU devices include an on-chip 2-Wire debug interface to allow Flash programming and simple debugging functions when used with ELAN IDE. The OCDS needs only a total of four pins as listed in Table 7-1.

OCDS pins	Function
VDD	Power
2W_SCL	Serial Clock
2W_SDA	Serial Data
VSS	Ground

Table 7-1 OCDS pin definition

7.1 Limitations of On-Chip Debug

During the debugging process, the user must be care of the 2W_SCL and 2W_SDA pins for data and clock communication purposes to ensure that no other components are connected to these two pins. A circuit components restriction is shown in Figure 7-1.

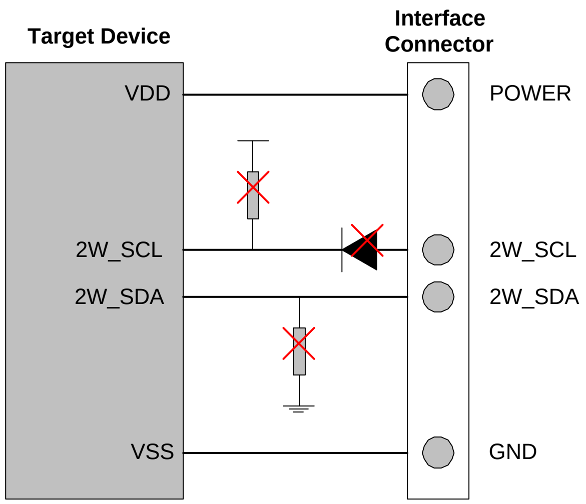


Figure 7-1 Diagram showing Circuit Components Restriction

Some guidelines to ensure efficient debugging:

1. Do not use pull-high and pull-down on the 2W_SCL/2W_SDA pin.

2. Do not use capacitors on the 2W_SCL/2W_SDA pin.

3. Do not use diodes on the 2W_SCL/2W_SDA pin.

During enter OCD mode process, the user must ensure signals are cleared on the 2W_SCL and 2W_SDA pins. If entering OCD mode is completed, the pin-shared function of 2W_SCL/2W_SDA will become invalid.

8 Timing Diagram

■ **AC Test Input / Output Waveform**

Note: *AC Testing**:** Input are driven at 2.4V for Logic "**1**" and 0.4V for Logic "**0**"*
*Timing measurements are made at 2.0V for Logic "**1**" and 0.8V for Logic "**0**"*

Figure 7-1 AC Test Input / Output Waveform Timing Diagram

■ **Reset Timing (CLK1:0 = "01")**

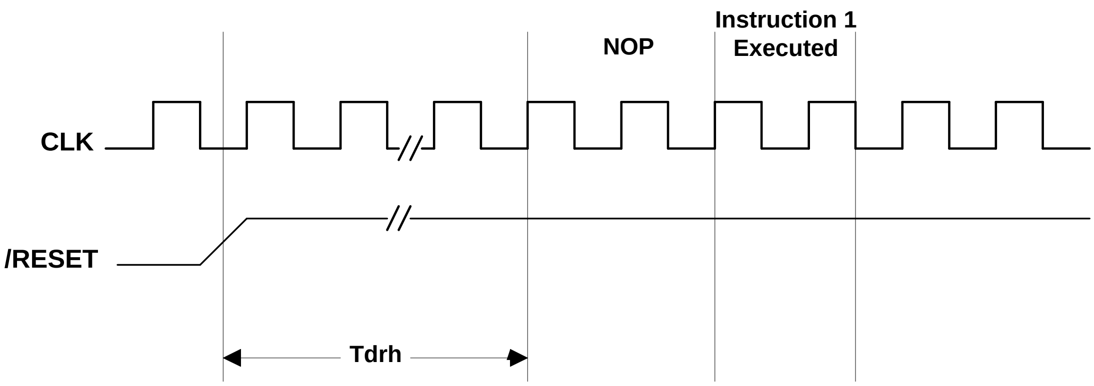


Figure 7-2 Reset Timing Diagram

9 Absolute Maximum Ratings

Items	Rating		
Temperature under bias	-40°C	to	85°C
Storage temperature	-65°C	to	150°C
Working voltage	2.2V	to	5.5V
Working frequency	DC	to	16 MHz
Input voltage	Vss-0.3V	to	Vdd+0.5V
Output voltage	Vss-0.3V	to	Vdd+0.5V

NOTE: *These parameters are theoretical values only and have not yet been verified.*

10 DC Electrical Characteristics

Ta=25°C, VDD=5.0V ± 5%, VSS=0V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Fxt	Crystal: VDD to 3V	Two cycles with two clocks	DC	–	8	MHz
	Crystal: VDD to 5V		DC	–	16	MHz
	ERC: VDD to 5V	R: 5.1KΩ, C: 300 pF	F-30%	185	F+30%	kHz
	IRC: 2.2V to 5V (IRC power is internal Regulator)	455KHz, 1 MHz (Ta = -40°C~85°C) (NUWriter Trim)	F-4%	F	F+4%	Hz
	IRC: 2.2V to 5V (IRC power is internal Regulator)	4 MHz, 8 MHz, 16 MHz (Ta = -40°C~85°C) (NUWriter Trim)	F-4.75%	F	F+4.75%	Hz
	IRC: 2.2V to 5V (IRC power is internal Regulator)	455KHz, 1 MHz (Ta = -40°C~85°C) (UWriter Trim)	F-4%	F	F+4%	Hz
	IRC: 2.2V to 5V (IRC power is internal Regulator)	4 MHz, 8 MHz, 16 MHz (Ta = -40°C~85°C) (UWriter Trim)	F-4.75%	F	F+4.75%	Hz
IIL	Input Leakage Current for input pins	VIN = VDD, VSS	-1	0	1	μA
VIHRC	Input High Threshold Voltage (Schmitt Trigger)	OSCI in RC mode	-	3.5	-	V
IERC1	Sink current	VI from low to high, VI=5V	21	22	23	mA
VILRC	Input Low Threshold Voltage (Schmitt Trigger)	OSCI in RC mode	-	1.5	-	V
IERC2	Sink current	VI from high to low, VI=2V	16	17	18	mA
VIH1	Input High Voltage (Schmitt Trigger)	Ports 5, 6, 8	0.7Vdd	-	Vdd+0.3V	V
VIL1	Input Low Voltage (Schmitt Trigger)	Ports 5, 6, 8	-0.3V	-	0.3Vdd	V

(Continuation)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VIHT1	Input High Threshold Voltage (Schmitt Trigger)	/RESET	0.7Vdd	-	Vdd+0.3V	V
VILT1	Input Low Threshold Voltage (Schmitt Trigger)	/RESET	-0.3V	-	0.3Vdd	V
VIHT2	Input High Threshold Voltage (Schmitt Trigger)	INT	0.7Vdd	-	Vdd+0.3V	V
VILT2	Input Low Threshold Voltage (Schmitt Trigger)	INT	-0.3V	-	0.3Vdd	V
IOH1	Output High Voltage (Ports 5, 6, 8)	VOH = 0.9VDD	-3.0	-4.2	–	mA
IOL1	Output Low Voltage (Ports 5, 8)	VOL = 0.1VDD	9	11	–	mA
IOL2	Output Low Voltage (Port 6)	VOL = 0.1VDD	15	18	–	mA
LVR1	Low voltage reset level	Ta= 25°C	2.2	2.5	2.8	V
LVR2	Low voltage reset level	Ta= 25°C	3.1	3.5	3.9	V
LVR3	Low voltage reset level	Ta= 25°C	3.6	4.0	4.5	V
IPH	Pull-high current	Pull-high active, Input pin at VSS	-	-70	-120	μA
IPL	Pull-low current	Pull-low active, Input pin at Vdd	-	20	50	μA
ISB1	Power down current (Sleep Mode)	All input and I/O pins at VDD, Output pin floating, WDT disabled	–	1	–	μA
ISB2	Power down current (Sleep Mode)	All input and I/O pins at VDD, Output pin floating, WDT enabled	–	5	–	μA
ICC1	Operating supply current at two clocks Normal Mode)	/RESET= 'High', Fosc=32kHz, HLP=Low (Crystal type, CLKS1:0="01"), Output pin floating, WDT disabled.	–	30	–	μA

(Continuation)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
ICC2	Operating supply current at two clocks Normal Mode)	/RESET= 'High', Fosc=32kHz, HLP=Low (Crystal type, CLKS1:0="01"), Output pin floating, WDT enabled.	–	31	–	µA
ICC3	Operating supply current at two clocks Normal Mode)	/RESET= 'High', Fosc=455kHz, HLP=Low (Crystal type, CLKS1:0="01"), Output pin floating, WDT enabled. (*VDD = 3V)	–	150	–	µA
ICC4	Operating supply current at two clocks Normal Mode)	/RESET= 'High', Fosc=455kHz, HLP=Low (IRC type, RCM1:0="11", IRE=Int. Regulator), Output pin floating, WDT disabled. (*VDD = 3V)	–	250	–	µA
ICC5	Operating supply current at two clocks Normal Mode)	/RESET = 'High', Fosc = 4 MHz, HLP=High (Crystal type, CLKS1:0 = "01"), Output pin floating, WDT enabled	–	1.1	–	mA
ICC6	Operating supply current at two clocks Normal Mode)	/RESET= 'High', Fosc=4MHz, HLP=High (IRC type, RCM1:0="00", IRE=Int. Regulator), Output pin floating, WDT enabled. (*VDD = 3V)	–	660	–	µA
ICC7	Operating supply current at two clocks Normal Mode)	/RESET = 'High', Fosc = 16 MHz, HLP=High (Crystal type, CLKS1:0 = "01"), Output pin floating, WDT enabled	–	4	–	mA
ICC8	Operating supply current at two clocks Normal Mode)	/RESET= 'High', Fosc=16MHz, HLP=High (IRC type, RCM1:0="01", IRE=Int. Regulator), Output pin floating, WDT enabled.	–	2.2	–	mA

NOTES:

1. *The above parameters are theoretical values only and have not yet been tested or verified. They are provided for design reference only.*
2. *Data under the "Min.", "Typ.", and "Max." (Minimum, Typical, and Maximum) columns are based on hypothetical results at 25°C.*

■ Data EEPROM Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Twrite	Write Cycle Time (Page/ byte write)	VDD = 2.0~ 5.5V Temperature = -40°C ~ 85°C	–	2	3	ms
Tall_write	Erase / Program Time (Write All)		–	5	6	ms
Tread	Read Time		100	–	–	ns
Trent	Data Retention		–	10	–	years
Tendur	Endurance time		–	100K	–	cycles

■ Program Flash Memory Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Tprog	Erase/Write cycle time	Vdd = 5.0V Temperature = -40°C ~ 85°C	–	1	1.5	ms
Treten	Data Retention		–	10	–	years
Tendu	Endurance time		–	100K	–	cycles

■ A/D Converter Characteristics Ta=25°C, VDD=5.0V ± 5%, VSS=0V

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Operating Range	Vdd	For 5.5v Fs=100KHz, Fin=1KHz, For 2.5v Fs=25KHz, Fin=1KHz	2.5	-	5.5	V
	V_{REFT}	-	2.5	-	Vdd	V
	V_{REFB}	-	Vss	-	$V_{REFT}-\Delta V_{REF}$	V
	ΔV_{REF}	-	2.5	-	-	V
1/2 VDD AD Input	$V_{1/2VDD}$	Vdd=5V	2.475	2.5	2.525	V
	$T_{1/2VDD}$	Vdd=5V	-	2.8	4	us
	$I_{1/2VDD}$	Vdd=5V	-	34.72	42	uA
Current Consumption	Ivdd	V_{REFT} = Vdd=5v, V reference from Vdd Fs=100KHz, Fin=1KHz	-	-	1	mA
	Iref		-	-	10	µA
	Ivdd	V_{REFT} = Vdd=5v, V reference from VREF Fs=100KHz, Fin=1KHz	-	-	0.6	mA
	Iref		-	-	0.4	mA
Standby Current	Isb	-	-	-	0.1	µA
ZAI	ZAI	-	-	-	10k	Ω
SNR	SNR	V_{REFT}= Vdd=5V Fs=100kHz, Fin=1kHz	70	-	-	dBc
THD	THD	V_{REFT}= Vdd=5V Fs=100kHz, Fin=1kHz	-	-	-70	dBc
SNDR	SNDR	V_{REFT}= Vdd=5V Fs=100kHz, Fin=1kHz	68	-	-	dBc
Worst Harmonic	WH	V_{REFT}= Vdd=5V Fs=100kHz, Fin=1kHz	-	-	-73	dBc

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
SFDR	SFDR	V_{REFT}= Vdd=5V Fs=100kHz, Fin=1kHz	73	-	-	dBc
Offset Error	OE	V_{REFT}= Vdd=5V Fs=100kHz	-	-	+/-4	LSB
Gain Error	GE	V_{REFT}= Vdd=5V Fs=100kHz	-	-	+/-8	LSB
DNL	DNL	V_{REFT}= Vdd=5V Fs=100kHz, Fin=1kHz	-	-	+/-1	LSB
INL	INL	V_{REFT}= Vdd=5V Fs=100kHz, Fin=1kHz	-	-	+/-4	LSB
Conversion Rate	Fs1	Vdd=3.0~5.5v, Fin=1kHz	-	-	100	KSPS
	Fs2	Vdd=2.5~3.0v, Fin=0.1kHz	-	-	25	KSPS
Power Supply Rejection Ratio	PSRR	V_{REFT}=2.5v, Vdd=2.5v ~ 5.5v, Fs=25K Hz, Vin=0v ~ 2.5v	-	-	2	LSB

NOTES:

1. *Fs is Sample Rate, that is to say, conversion rate. Fin is freq. of input test sine wave*
2. *The parameters are theoretical values and have not yet been tested. Such parameters are for design reference only*
3. *There is no current consumption when ADC is off other than minor leakage current.*
4. *AD conversion result will not decrease when the input voltage increased, and there is no missing code.*
5. These parameters are subject to change without further notice.

■ Comparator Electrical Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating Range	Vdd		2.5	–	5.5	V
Current Consumption	Ivdd	Vdd=5.5V Without bandgap	150	200	250	uA
Input offset voltage	Vos	trimming at 25℃,operaing at 25℃	-2		2	mV
TRS	Response time	trimming at 25℃,operaing at -40~105℃	-8	–	8	µs
Input common mode range	Vcm	Vdd=5	0	–	vdd	V
Warn up time	Twu		–	10	–	us
Response time	Trs	Vdd＝5V 100mV input step with 10mV overdrive CL=10pF	300	400	500	ns

11 AC Electrical Characteristics

- **0 ≤ Ta ≤ 70°C, VDD=5V, VSS=0V**
- **–40 ≤ Ta ≤ 85°C, VDD=5V, VSS=0V**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Dclk	Input CLK duty cycle	–	45	50	55	%
Tins	Instruction cycle time (CLKS1:0="01")	Crystal type	100	–	DC	ns
		RC type	500	–	DC	ns
Ttcc	TCC input period	–	(Tins+20)/N*	–	–	ns
Tdrh	Device reset hold time	–	14	16	18	ms
Trst	/RESET pulse width	Ta = 25°C	2000	–	–	ns
Twdt	Watchdog timer period	Ta = 25°C VDD = 2.2~ 5.5V	16-9%	16	16+9%	ms
Tset	Input pin setup time	–	–	0	–	ns
Thold	Input pin hold time	–	–	20	–	ns
Tdelay	Output pin delay time	Cload = 20 pF	–	50	–	ns

***N** = *Selected prescaler ratio*

NOTES:

1. The above parameters are theoretical values only and have not yet been tested or verified. They are provided for design reference only.

2. Data under the “Min.”, “Typ.” and “Max.” (Minimum, Typical, and Maximum) columns are based on hypothetical results at 25℃.

APPENDIX

A Ordering and Manufacturing Information

EM78F811NMS10J

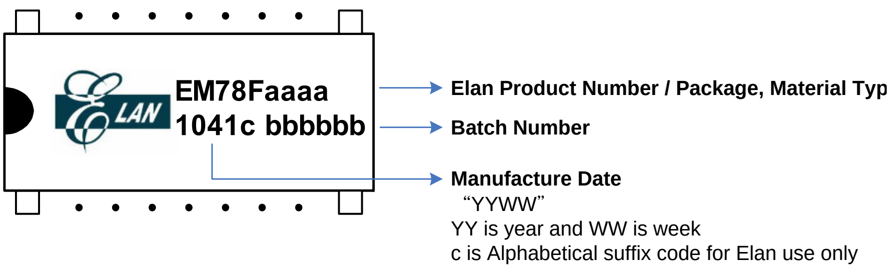
- **Material Type**
  J: RoHS complied
  S: Sony SS-00259 complied
  Contact Elan Sales for details
- **Pin Number**
- **Package Type**
  D: DIP
  SO: SOP
  MS: MSOP
  Check the following section for details
- **Specific Annotation**
- **Product Number**
- **Product Type**
  N: FLASH
- **Elan 8-bit Product**

For example:

EM78F811NMS10J

is EM78F811N with FLASH program memory, product, in 10-pin DIP 118mil package with RoHS complied

IC Mark



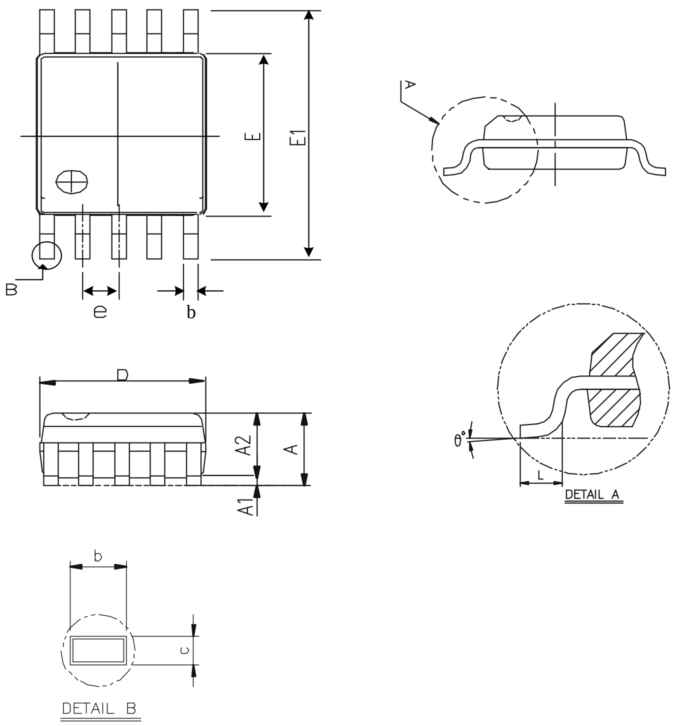
B Package Type

Flash MCU	Package Type	Pin Count	Package Size
EM78F811NMS10	MSOP	10	118 mil
EM78F811NSO14	SOP	14	150 mil
EM78F811NAD16	DIP	16	300 mil
EM78F811NASO16A	SOP	16	150 mil

Part No.	EM78F811NxJ/xS
Electroplate type	Pure Tin
Ingredient (%)	Sn: 100%
Melting point (°C)	232°C
Electrical resistivity (µΩ cm)	11.4
Hardness (hv)	8~10
Elongation (%)	>50%

C Packaging Configuration

C.1 EM78F811NMS10



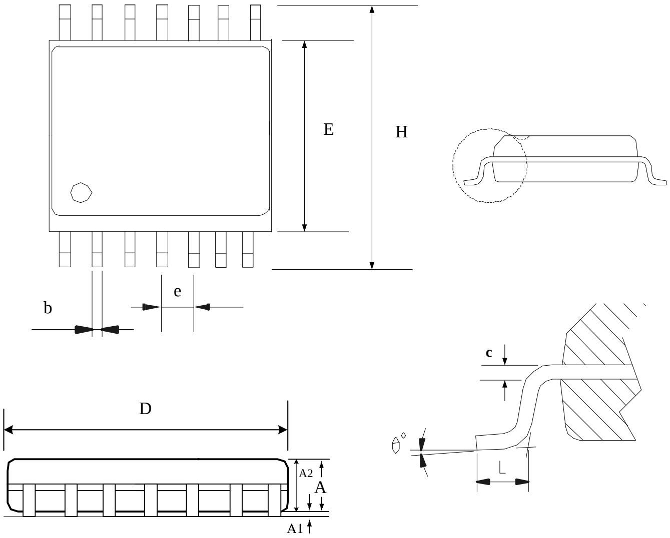
Symbal	Min	Normal	Max
A			1.1
A1	0.05		0.15
A2	0.75	0.85	0.95
D	2.90	3.00	3.10
E	2.90	3.00	3.10
E1	4.7	4.9	5.1
b	0.19		0.28
c	0.15		0.2
L	0.4		0.7
e	0.5BSC		
θ	0°	-	8°

TITLE:
MSOP 10L (118MIL)PACKAGE OUTLINE DIMENSION

File : MSOP 10 L | Edtion: A
Unit : mm
Scale: Free
Material:
Sheet:1 of 1

Figure C-1 EM78F811N10-pin MSOP Package Type

C.2 EM78F811NSO14



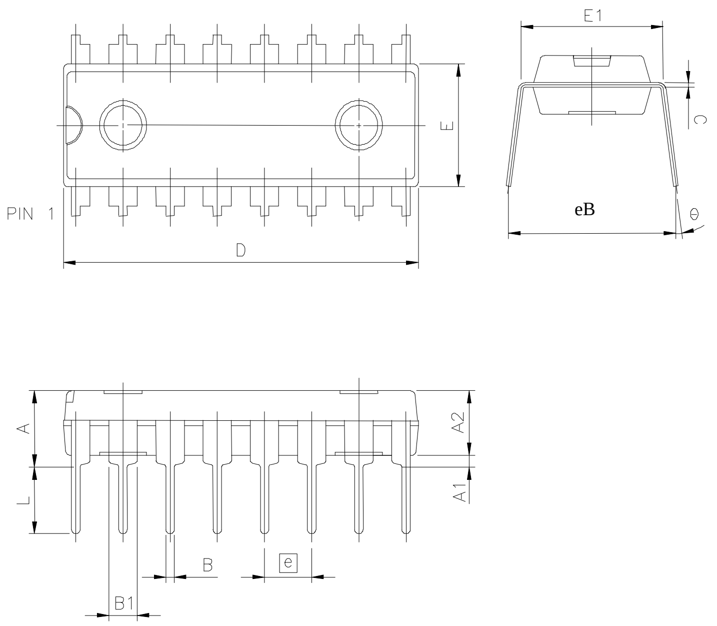
Symbol	Min	Normal	Max
A	1.350		1.750
A1	0.100		0.250
b	0.330		0.510
c	0.190		0.250
E	3.800		4.000
H	5.800		6.200
D	8.550		8.750
L	0.600		1.270
e	1.27(TYP)		
θ	0		8

TITLE:
SOP-14L(150MIL) PACKAGE OUTLINE DIMENSION

File : NSO14	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

Figure C-2 EM78F811N14-pin SOP Package Type

C.3 EM78F811NAD16

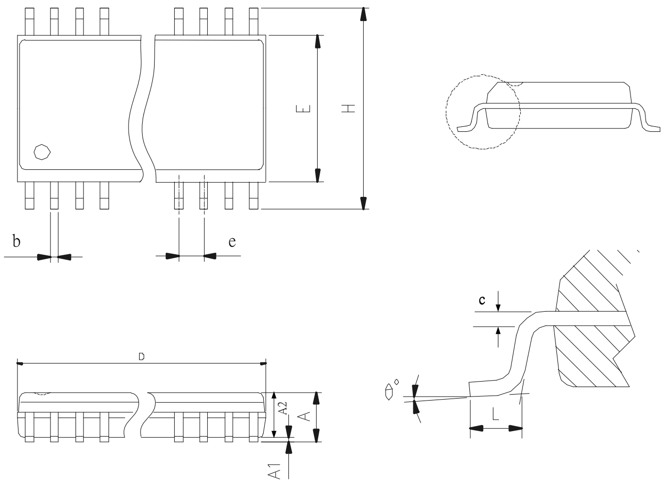


Symbal	Min	Normal	Max
A			4.318
A1	0.381		
A2	3.175	3.302	3.429
c	0.203	0.254	0.356
D	19.000	19.050	19.100
E	6.174	6.401	6.628
E1	7.370	7.620	7.870
eB	8.510	9.020	9.530
B	0.356	0.457	0.559
B1	1.143	1.524	1.778
L	3.048	3.302	3.556
e	2.540(TYP)		
θ	0		15

TITLE: PDIP-16L 300MIL PACKAGE OUTLINE DIMENSION	
File : D16	Edtion: A
ELAN	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

Figure C-3 EM78F811N16-pin DIP Package Type

C.4 EM78F811NASO16A



Symbol	Min.	Normal	Max.
A	1.350		1.750
A1	0.100		0.250
A2	1.300	1.400	1.500
b	0.330		0.510
c	0.190		0.250
E	3.800		4.000
H	5.800		6.200
D	9.800		10.000
L	0.600		1.270
e	1.27 (TYP)		
θ°	0		8

TITLE: SOP-16L(150MIL) PACKAGE OUTLINE DIMENSION	
File : NSO16	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

Figure C EM78F811N 16-pin SOP Package Type

D Quality Assurance and Reliability

Test Category	Test Conditions	Remarks
Solderability	Solder temperature=245±5°C, for 5 seconds up to the stopper using a rosin-type flux	–
Pre-condition	**Step 1:** TCT, 65°C (15 min)~150°C (15 min), 10 cycles	For SMD IC (such as SOP, QFP, SOJ, etc)
	Step 2: Bake at 125°C, TD (endurance)=24 hrs	
	Step 3: Soak at 30°C/60%，TD (endurance)=192 hrs	
	Step 4: IR flow 3 cycles (Pkg thickness ≥ 2.5 mm or Pkg volume ≥ 350 mm^3 ----225±5°C) (Pkg thickness ≤ 2.5 mm or Pkg volume ≤ 350 mm^3 ----240 ± 5°C)	
Temperature cycle test	-65°C (15 min)~150°C (15 min), 200 cycles	–
Pressure cooker test	TA =121°C, RH=100%, pressure=2 atm, TD (endurance)= 96 hrs	–
High temperature / High humidity test	TA=85°C , RH=85%，TD (endurance) = 168 , 500 hrs	–
High-temperature storage life	TA=150°C, TD (endurance) = 500, 1000 hrs	–
High-temperature operating life	TA=125°C, VCC = Max. operating voltage, TD (endurance) = 168, 500, 1000 hrs	–
Latch-up	TA=25°C, VCC = Max. operating voltage, 150mA/20V	–
ESD (HBM)	TA=25°C, ≥ ｜± 3KV｜	IP_ND,OP_ND,IO_ND IP_NS,OP_NS,IO_NS IP_PD,OP_PD,IO_PD, IP_PS,OP_PS,IO_PS, VDD-VSS(+),VDD_VSS (-) mode
ESD (MM)	TA=25°C, ≥ ｜± 300V｜	

D.1 Address Trap Detect

Address Trap Detect is one of the MCU embedded fail-safe functions that detects MCU malfunction caused by noise or the like. Whenever the MCU attempts to fetch an instruction from a certain section of ROM, an internal recovery circuit will automatically start. If a noise-caused address error is detected, the MCU will repeat execution of the program until the noise is eliminated. The MCU will then continue to execute the next program.